Local Gate Control in Carbon Nanotube Quantum Devices

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by

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Abstract

This thesis presents transport measurements of carbon nanotube electronic devices operated in the quantum regime. Nanotubes are contacted by source and drain electrodes, and multiple lithographically-patterned electrostatic gates are aligned to each device. Transport measurements of device conductance or current as a function of local gate voltages reveal that local gates couple primarily to the proximal section of the nanotube, hence providing spatially localized control over carrier density along the nanotube length. Further, using several different techniques we are able to produce local depletion regions along the length of a tube. This phenomenon is explored in detail for different contact metals to the nanotube.

We utilize local gating techniques to study multiple quantum dots in carbon nanotubes produced both by naturally occurring defects, and by the controlled application of voltages to depletion gates. We study double quantum dots in detail, where transport measurements reveal honeycomb charge stability diagrams. We extract values of energy-level spacings, capacitances, and interaction energies for this system, and demonstrate independent control over all relevant tunneling rates.

We report rf-reflectometry measurements of gate-defined carbon nanotube quantum dots with integrated charge sensors. Aluminum rf-SETs are electrostatically coupled to carbon nanotube devices and detect single electron charging phenomena in the Coulomb blockade regime. Simultaneous correlated measurements of single electron charging are made using reflected rf power from the nanotube itself and from the rf-SET on microsecond time scales. We map charge stability diagrams for the nanotube quantum dot via charge sensing, observing Coulomb charging diamonds beyond the first order.

Conductance measurements of carbon nanotubes containing gated local depletion regions exhibit plateaus as a function of gate voltage, spaced by approximately $1e^2/h$, the quantum of conductance for a single (non-degenerate) mode. Plateau structure is investigated as a function of bias voltage, temperature, and magnetic field. We speculate on the origin of this surprising quantization, which appears to lack band and spin degeneracy.

Contents

List of Figures

Citations to Previously Published Work

Nearly all of the experimental results presented in this thesis have appeared in refereed journals, while some have been submitted for publication and can be found as preprints on the cond-mat archive.

The fabrication details (Section 3.2.1) and transport measurements (Appendix B) presented in this thesis appear in the following article:

> "Local Gating of Carbon Nanotubes", M. J. Biercuk, N. Mason, C. M. Marcus, *Nano Lett.* **4**, 1 (2004).

Chapter 5 appears in its entirety as:

> "Local Gate Control of a Carbon Nanotube Double Quantum Dot", N. Mason, M. J. Biercuk, C. M. Marcus, *Science* **303**, 655 (2004).

The majority of Chapter 6 appears as:

> "Locally Addressable Tunnel Barriers within a Carbon Nanotube", M. J. Biercuk, N. Mason, J. M. Chow, C. M. Marcus, *Nano Lett.* **4**, 2499 (2004).

Most of Chapter 7 appears as:

> "Gate-Defined Quantum Dots on Carbon Nanotubes", M. J. Biercuk, S. Garaj, N. Mason, J. M. Chow, C. M. Marcus, `cond-mat/0502634`. In press, *Nano Lett.* (2005).

Section 8.2, the last set of experiments performed for this thesis while I was in Sydney, Australia will soon appear as:

> "Single Charge Detection in Carbon Nanotube Quantum dots on microsecond timescales", M. J. Biercuk, D. J. Reilly, T. M. Buehler, V. M. Chan, J. M. Chow, R. G. Clark, C. M. Marcus, To be submitted.

The experimental results of Section 9.2 appear as:

> "Anomalous Conductance Quantization in Carbon Nanotubes", M. J. Biercuk, N. Mason, J. Martin, A. Yacoby, C. M. Marcus, *Phys. Rev. Lett.* **94**, 026801 (2005).

Finally, the processing techniques developed for the deposition, patterning and characterization of low-temperature atomic layer deposition oxide films appearing in Appendix A also appear as:

> "A Low-Temperature Atomic Layer Deposition Liftoff Method for Microelectronic and Nanoelectronic Applications", M. J. Biercuk, D. J. Monsma, C. M. Marcus, J. S. Becker, R. G. Gordon, *App. Phys. Lett.* **83**, 2405 (2003).

Electronic preprints (shown in `typewriter font`) are available on the Internet at the following URL:

> `http://arXiv.org`

In addition to the publications listed above, I've also been fortunate enough to have presented a number of invited talks and seminars on my work over the past several years. Some of those are listed here:

- Invited Seminar: National Cancer Institute Nanotechnology Seminar, 18 May, 2005.
- Invited Seminar: DARPA Microsystems Technology Office, 10 May, 2005.
- Invited Seminar: Harvard NSEC Research Exchange Seminar, 19 April, 2005.
- Invited Talk: APS March Meeting, 22 March 2005.
- Invited Seminar: Univ. of New South Wales, School of Physics Nanotechnology course, 2 March 2005.
- Invited Talk: Centre for Quantum Computer Technology Workshop, Avoca Beach, Australia, 10 Feb 2005.
- Invited Seminar: Univ. of New South Wales, 18 Jan 2005.
- Invited Talk: ARDA/NSA, 16 November 2004.
- Invited Seminar: Stanford Condensed Matter Seminar, 21 October, 2004.
- Invited Seminar: Harvard Condensed Matter Theory Kids Seminar 2004.

Acknowledgments

Writing the acknowledgements section of a thesis is supposed to be the easiest part—that's why it's always saved for last. It's not entirely clear that I can write a few paragraphs and sufficiently express my gratitude to all those who made this thesis possible. I shall do my best.

It's necessary that I begin with my PhD advisor, Charlie Marcus (Prof. Charles M. Marcus). Graduate school is a challenging and formative time in a young scientist's life. I thank Charlie for his part in making my graduate experience both. Like any graduate student, the happiness of my experience on any given day was strongly correlated to how experiments were proceeding. Looking back, however, I realize how incredibly fortunate I am to have worked with Charlie. The science in the Marcus lab is incredibly exciting, as are the new ideas constantly offered by Charlie and the steady stream of world-class researchers coming through the lab. I most enjoyed, however, learning to be a *scientist* from Charlie—learning a method for approaching any given problem which carries over into all areas of life. I'm thankful for his support, his encouragement and the motivation he supplied to make me aim higher.

I'm also particularly indebted to my research partner for much of my time in graduate school, Nadya Mason, now a professor at UIUC. Nadya taught me everything from low-noise transport measurement techniques to cryogenics and I owe much of my technical knowledge to her. I'm grateful to Nadya for teaching me, putting up with me, and being a friend, no matter the circumstances. She has been a role-model to me, and I'm certain she will have as much of an impact on many other students while running her own lab.

My many lab mates made my time at Harvard tremendously enjoyable. Alex has my thanks for his frightening ability to see through any physics problem, his love of meat, his penny-shooting-prowess, and his friendship. The sheer quantity of ice cream,cold cuts and chocolate syrup that I owe Alex could fill a shielded room. Likewise, I'm proud to have worked with Ron Potok, who despite his move to Stanford, remains a good friend and a gifted colleague. I had the pleasure of working with two fantastic undergraduates during my time here - Jerry Chow and Will Koehl. Both will certainly go on to great things, despite my corrupting influence. Jason Petta, superstar, had a huge influence on the group and on my pecs. He has been a great friend and lifting partner and I'm looking forward to his next scientific revolution. I'm thankful to Douwe Monsma for his tremendous input while I was developing fabrication techniques in the lab. He truly has an encyclopedic knowledge of materials and device physics, and without his assistance we would have been dead in the water. I must also thank all of the other students and postdocs with whom I've had the pleasure of working—Leo DiCarlo (the "GG"), Yiming Zhang, Doug McClure (neep), Jeff Miller, Dominik Zumbuhl, Edward Laird, Nathaniel Craig (possibly the most kind-hearted person I've ever met), Bart Horn, Slaven Garaj and Susan Watson.

Being at Harvard also allowed me to interact with other fantastic researchers in the McKay building. My thanks to Nina Markovic, Sergio Valenzuela, Steven Cronin, William Neils and John Free from the Tinkham lab. Also, Ania Bleszynski, Parisa Fallahi, Tom Hunt, Hakho Lee and Ian Chan in the Westervelt group. Similarly, I'm thankful to all of the Professors at Harvard from whom I've taken classes or simply interacted scientifically. My thanks to Professors Eugene Demler, Bert Halperin, Misha Lukin, David Nelson, Rick O'Connell and Bob Westervelt.

The many hours I've spent in the Harvard cleanrooms (AKA Yellow Hell) often drove me to the brink of insanity. I managed to avoid that abyss thanks to the tremendous technical support of David Bell, Yuan Lu, Steve Shepard and John Tsakirgis.

During the winter of 2005, I had the privilege to work at the University of New South Wales in Sydney, Australia. It was, honestly, one of the best experiences of my life. I met many wonderful people in the Centre for Quantum Computer Technology who made my visit a wonderful experience. Dave Barber, Matt Butcher, Marty Brauhart, Rolf Brenner, Nadia Court, Neil Curson, Andrew Ferguson, Bob Starrett, and Thilo Reusch all made me feel amazingly welcome. The snorkeling trips with Matt, Thilo and Marty were particularly enjoyable. Naturally, I thank R. Kanga and Strongbad for technical support, useful discussions and wondrous visuals. Of course, I owe a great deal to Tilo Buehler, Victor Chan and David Reilly, with whom I worked closely during my visit. I'm particularly indebted to David for all of his help organizing my visit, his scientific input and his friendship. It's a tremendous pleasure having him in the Marcus Lab as a postdoc now, and I look forward to future collaborations. My thanks also go to Prof. Bob Clark for supporting my visit to the Centre.

I'm grateful to Peter Jackson for making the films which carried me through graduate school. You've entertained and touched more people than you know.

Finally I'd like to thank the people who have mattered most in this endeavor. I owe everything to my parents for their love and support, even when I was too busy to visit. Although there were often many months between visits, they were never out of mind. And to my future wife, Anna. Thank you for believing in me and for giving me your heart. You have made every day worthwhile...

To my parents,
and Anna.

Chapter 1

Introduction

1.1 Motivation

"There's plenty of room at the bottom," the portentous 1959 talk [52] presented by Richard Feynman looking towards the future of physics, guides (in an indirect way) much of the research currently being pursued in experimental condensed matter and chemical physics. "What I want to talk about is the problem of manipulating and controlling things on a small scale." This simple statement has in some regards become the foundation of the nascent and rapidly developing field of nanotechnology, in which scientists aim to manipulate, design, and control devices at the atomic level [48]. Feynman continued, "At the atomic level, we have new kinds of forces and new kinds of possibilities, new kinds of effects." Despite a tremendous amount of hype and spin flying about in the press regarding nanotechnology, the previous statement captures an essential component of nanotech which is generally overlooked. While with the use of nanotechnology one might produce a better paint, or a more efficient transistor, or stronger composite materials, the great promise of nanotechnology lies in those applications that rely on fundamentally “new kinds of effects.”

Nanotechnology is a term broadly used to label fields of scientific inquiry focused on materials systems whose size scale (in at least one dimension) is on the order of nanometers (nanotechnology being eponymous with the prefix $nano = 10^{-9}$). There are official definitions of what constitutes nanotechnology, mainly employed as a distinction for research funding agencies, but it is generally accepted that research in submicron electronic devices may be considered nanotech. It is worth noting that the addition of the suffix “-technology” to the name of the field at large should not necessarily imply that research is only applied in nature.

Among those researchers in the field of “nanoelectronics” at the present time, there seem to be two prevailing approaches to the problem of building nanoscale electronic devices: bottom-up and top-down. The bottom-up approach focuses on the controlled synthesis of nanoscale structures from a “blank slate,” while top-down seeks to build nanoscale components starting with bulk materials such as Si or GaAs wafers and appropriate processing techniques. Naturally, key players in both camps (who shall remain nameless) believe that their approach is—with mutual exclusivity—the correct one to pursue.

As with all great ideological divides, the truth (in this case the usefulness of a technique) lies somewhere in the middle. Accordingly, this thesis will discuss nanoscale electronic devices which are fabricated using a combination of top-down and bottom-up techniques. It will explore the “new possibilities” and “new kinds of effects” found only at the nanoscale, where quantum mechanics strongly influences phenomena as familiar as electrical conductance.

The experiments described in this thesis focus on electron transport measurements performed on carbon nanotubes. Much of the work presented here will describe technological advancements we have made in order to produce electronic devices from carbon nanotubes with functionality similar to those which have been fabricated in two-dimensional electron systems for over a decade. These advancements have largely come in the realm of producing local electrostatic gates on single nanotubes, and in that respect borrow heavily from the top-down community of researchers. We are not, however, patterning conducting channels from a semiconductor heterostructure; instead we utilize a molecular form of carbon grown synthetically *in situ* as the fundamental unit of our devices – a decidedly bottom-up approach.

While the transport measurements presented in this thesis stand on their own, there is a unifying theme to all of the experiments presented herein. Our work has aimed to provide carbon nanotube devices the necessary functionality for applications in coherent electronics. While little of the work presented here will deal with quantum mechanical phase coherent processes, it has been performed in preparation for more advanced measurements in which such processes will be studied. For example, measurements of the interactions between two phase-coherent, isolated spins in a carbon nanotube require techniques to independently control both spins. This work has focused on providing the necessary technical infrastructure to the field in order to facilitate a move towards useful coherent logic applications employing carbon nanotubes.

1.2 Organization of this Thesis

Despite a clear focus on technology, the work presented in this thesis relies heavily on both the basic physics of electron transport in low-dimensional structures as well as device and semiconductor physics. In the midst of the technical journey taken to build these devices we made several fundamental physics pit-stops which will be described in detail and will be prefaced by adequate background material and discussion. Although many technical advances follow one another in chronological order, there are several places where chronology will be trumped by a logical organization which suggests that some work stand independent of other experimental achievements.

A natural place to begin is with carbon nanostructures, including detailed discussions of the structure and electrical properties of carbon nanotubes—the fundamental component of the devices detailed in these experiments. Chapter 2 will continue with a discussion of previous measurements of carbon nanotube electronic devices, and a presentation of the state of the art in the field at the time the work presented in this thesis began.

After introducing carbon nanotubes and providing background material on previous experiments, I will continue with a discussion of fabrication techniques employed in our lab in chapter 3. This chapter will include a description of the various local gating techniques we developed and employed in our experiments. These approaches include the growth of carbon nanotubes across pre-defined metal gates (“undergating”), laterally aligning gates to carbon nanotubes (“sidegating”), and lithographically aligning gates to carbon nanotubes buried under an insulating dielectric layer (“topgating”).

Chapter 4 will introduce in detail the concept of single electron charging in isolated puddles of electrons known as quantum dots. The transport characteristics of single and double quantum dots will be presented, and previous experiments discussed.

Chapter 5 will present transport measurements demonstrating local gate control in carbon nanotube double quantum dots using a top-gated geometry; top-gating being the most successful and robust technique employed in our work. The device described in this section relies upon naturally occurring (and minimally controllable) tunnel barriers at the metal-nanotube interface and in the middle of the tube itself.

Subsequently, in Chapter 6, I will describe our efforts to produce controllable tunnel barriers in the middle of carbon nanotubes via mechanical deformation using an atomic force microscope tip. Transport measurements indicating a preferential gating effect on the mechanically deformed sections of the nanotube will be presented. A comparison between tubes contacted with Schottky contacts and those ohmically contacted will be made.

Chapter 7 will describe the next generation of intratube quantum dots defined and controlled solely by the application of electrostatic gate voltages when nanotubes are contacted ohmically. Transport measurements of single and double dots fabricated in this manner will be presented and analyzed in detail. A comparison of dielectric materials for applications in nanotube top-gated devices will be presented.

Next, capacitive charge detection will be introduced and other experiments in which charge detection or "listening" was employed will be discussed. I will then briefly introduce the concepts of rf-reflectometry, impedance matching networks, wavelength division multiplexing and the characteristics and operation of the radio-frequency single electron transistor (rf-SET) for applications in ultra-sensitive electrometry, all in the first section of Chapter 8. Following this introduction, I will describe the fabrication of, and recent measurements on, gate-defined intratube quantum dots with integrated Al rf-SETs. Transport measurements demonstrating capacitive charge sensing of single electron addition on microsecond time-scales will be presented.

In the final chapter of this thesis, Chapter 9, I will present background theory on the phenomenon of 1D transport. The Landauer formalism, giving rise to the now familiar conductance quantum, will be introduced, and transport measurements on 1D systems discussed. This will be followed by the presentation of transport measurements on carbon nanotubes with ohmic contacts and locally gated intratube depletion regions. A surprising observation emerged from these experiments; namely the appearance of conductance plateaus spaced by the nondegenerate conductance quantum, e^2/h. Possible mechanisms leading to this observation will be discussed.

At the conclusion of this thesis I will present two useful appendices on such topics as low-temperature atomic layer deposition and patterning of thin film dielectrics in Appendix A, and transport measurements on undergated nanotube devices (Appendix B).

Chapter 2

Carbon nanotubes

2.1 Nanotube structure

Observations of crystalline molecular forms of carbon existing distinct from the familiar diamond and graphite began in 1985 [95] with the discovery of nanoscale carbon molecules later named fullerenes, the most famous of which is the C_{60} molecule. A few years later, in 1991, Professor Iijima discovered what he called carbon "microtubules," which turned had a molecular structure similar to that of an elongated fullerene [78]. Today such structures are widely recognized by the name "Carbon Nanotubes."

The structure of carbon nanotubes is derived from that of the graphene sheet, the 2D building block of 3D graphite. In graphene, carbon atoms are arranged on a hexagonal bravais lattice with a 2-atom basis yielding what is commonly known as a honeycomb lattice. Carbon nanotubes share the honeycomb structure of carbon bonds possessed by graphene, but, as their name suggests, do not exist in a planar

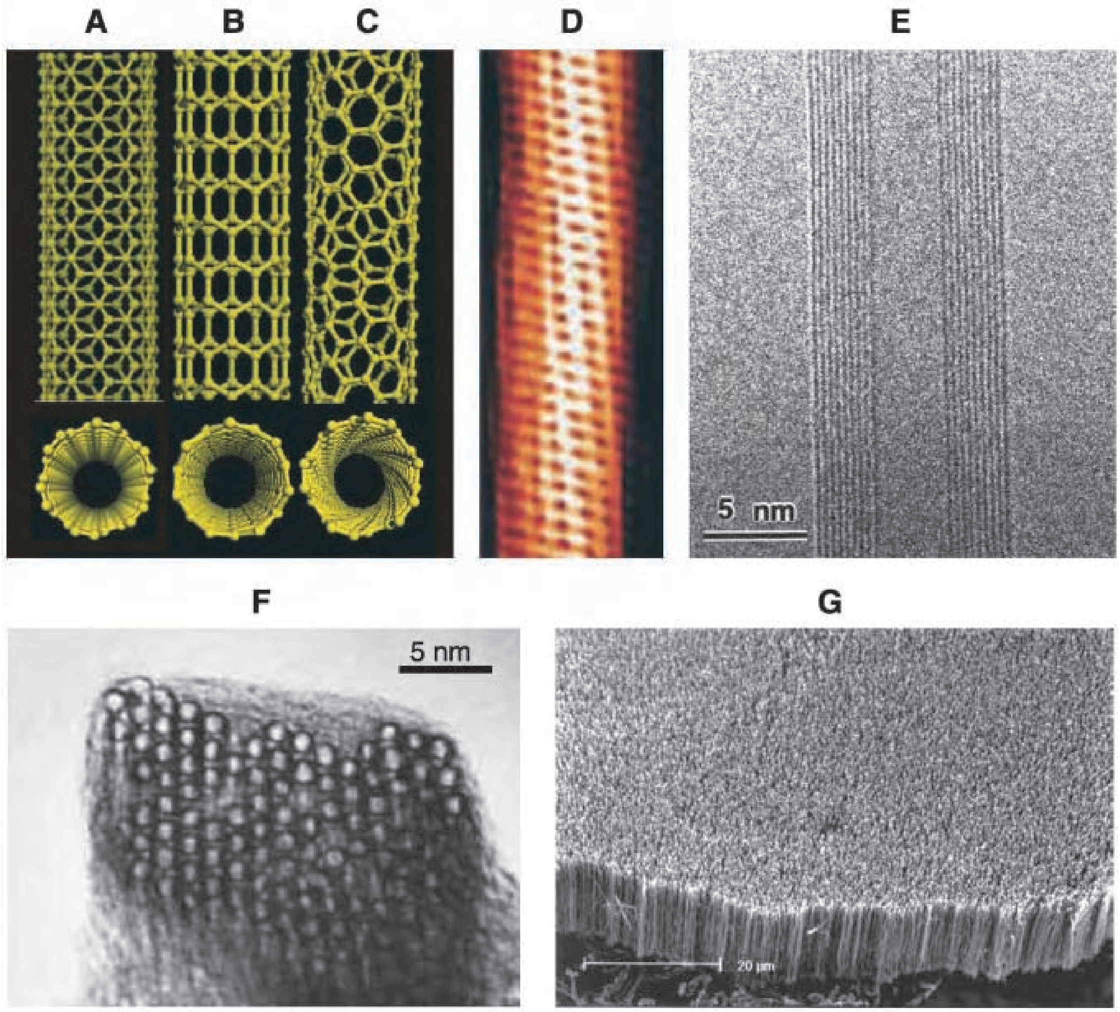

Figure 2.1: Various representations of carbon nanotube structure, adapted from [15]. Panels A, B, and C show schematics of armchair, zigzag and chiral nanotubes. D)STM image of chiral nanotube. E) TEM of a multiwalled nanotube showing multiple carbon shells. F) Cross-sectional TEM of a nanotube rope showing multiple tubes in a close-packed configuration. G) SEM of a MWNT nanotube forest.

structure. Rather, nanotubes may be thought of as a 2D graphene sheet which has been rolled-up onto itself to form a cylindrical structure with a diameter typically ∼1–5 nm . There is an additional complication as well: the manner in which the sheet is rolled up produces nanotubes with dramatically different geometrical configurations, a property called chirality. Starting with the graphene sheet, one may arbitrarily choose any two lattice sites to be connected when forming the nanotube structure. Such a scenario is demonstrated in Fig. 2.4 and labeled by the wrapping vector $\vec{w} = n\vec{a_1} - m\vec{a_2}$, where $\vec{a_1}$ and $\vec{a_2}$ are the primitive translation vectors of the hexagonal lattice and the prefactors n and m are integers. Hence the wrapping vector labels the number of primitive translation vectors one must move circumferentially from the origin to return to the same point on the cylinder. Accordingly, tubes are generally labeled by their wrapping vectors as (n, m): $(n, 0)$ are generally called “armchair,” and have carbon bonds perpendicular to the long axis of the nanotube (Fig. 2.1a); (n, n) tubes are called “zigzag” and have carbon bonds parallel to the longitudinal axis of the tube (Fig. 2.1b); all remaining (n, m) configurations are referred to as chiral (Fig. 2.1c). With atomic resolution this structure has been observed via scanning tunneling microscopy, as in Fig. 2.1d.

Nanotubes need not possess only a single outer wall, however. Thus we distinguish between single-walled nanotubes (SWNTs) and multi-walled nanotubes (MWNTs) which possess many concentric shells around a common core. High-resolution transmission electron microscopy can reveal these multiple shells in images such as Fig. 2.1e. In contrast, another nanotube supermolecular structure distinct from the MWNT exists in the form of a SWNT rope, similar to a bunching of soda straws into a close-packed lattice (Fig. 2.1f).

2.2 Electronic properties

At this point, carbon nanotubes as a material system are relatively well-understood. Accordingly, I will present only a few of the salient properties of carbon nanotube band structure, directing the reader to reference [138] for an incredibly detailed and useful treatment of the topic.

2.2.1 Graphene

Starting with graphene, the two-dimensional sheet of carbon atoms from which nanotubes are derived, one notes that due to the planar arrangement of carbon-carbon σ-bonds (each carbon atom is bonded to three others) the carbon atoms are in an sp^2 electronic configuration. This leaves one free electron per atom in a p_z orbital, perpendicular to the plane of the graphene sheet. Graphene band structure may be calculated using a tight-binding formulation which considers only the electrons in the p_z orbitals, and ignores any influence of the sp^2 electrons [161].

The Brillouin zone of graphene is hexagonal and contains two nonequivalent K-points, as there are two carbon atoms per unit cell of the Bravais lattice. It is straightforward to show that the band structure derived from tight-binding mirrors these symmetries as represented in Fig. 2.2. Further, the symmetric and antisymmetric combinations of atomic orbitals leads to bonding (π) and antibonding (π^*) orbitals which cross at the Fermi level. At this energy, the density of states vanishes. Normally, a material with two electrons per unit cell behaves as an insulator, but

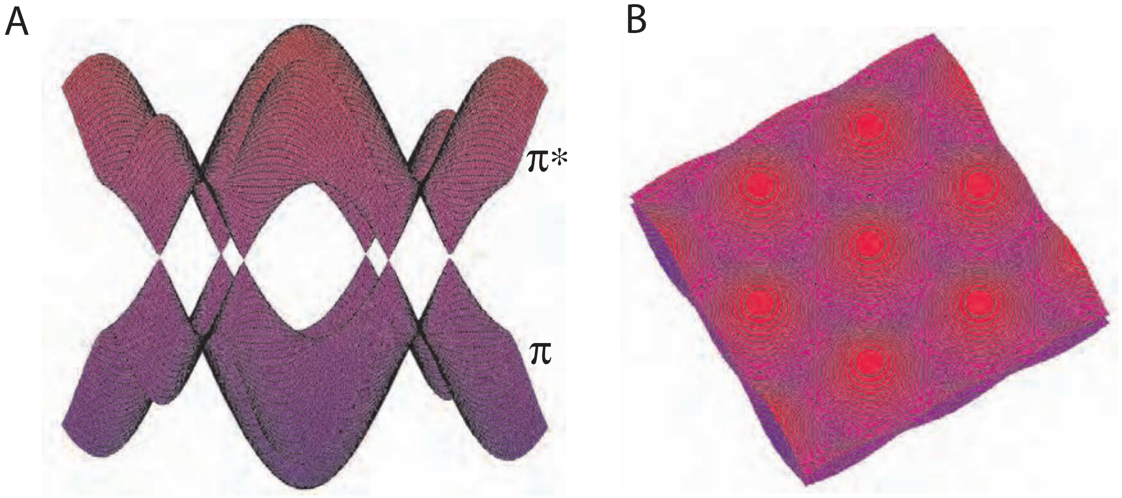

Figure 2.2: Band structure of graphene as calculated using the tight-binding approximation. A) Side view of the π and π^* bands crossing at the Fermi level. The Fermi surface of graphene consists of the six points of intersction. B)The hexagonal symmetry of the graphene sheet is plainly visible in this top-view of the calculated bandstructure. Calculation produced with Maple.

graphene, due to the band-crossing at the Fermi level behaves, and is classified, as a semimetal.

Semimetals, more generally, are materials with a small band overlap near the Fermi Level, such that a nonzero carrier population exists in the upper band. Graphene does not have band overlap, but does have (in the absence of external doping) an equal number of thermally excited carriers (electrons in the conduction band and holes in the valence band) in each band.

2.2.2 Nanotubes

The band structure of graphene provides the foundation for that of carbon nanotubes. In fact, the only difference between the two arises because of the imposition of periodic boundary conditions on the momentum wavevector perpendicular to the tube axis, $\vec{k_\perp}$. This leads to a quantization of $\vec{k_\perp}$ after fulfilling the condition $\vec{k} \cdot \vec{w} = 2\pi q$, where $\vec{w}$ is the wrapping vector and q is an integer. Hence, the spacing between allowed values of the transverse momentum vector satisfies the relationship $\Delta\vec{k_\perp} = 2/d$, with d the tube diameter. In reciprocal space this can be represented as a series of lines spaced by $\Delta\vec{k_\perp}$ traversing the Brillouin zone, representing the allowed wavevectors.

The form of the 1D subbands of a nanotube are determined by taking 1D slices of the graphene band structure represented in Fig. 2.2. Under certain conditions (Fig. 2.3), the allowed $\vec{k}$ fall directly on the K-points of the graphene Brillouin zone. Recalling that these points constitute the Fermi surface of graphene, the 1D dispersion relation $E(\vec{k_{||}})$ for the nanotube (1D slices through the graphene bandstructure) yields bands which cross at the Fermi level, and hence metallic behavior. If instead the allowed $\vec{k}$ do not cross the K-points the $E(\vec{k_{||}})$ has a gap around the Fermi level and hence the tube will behave as a semiconductor [119, 69, 139]. The resulting band structure of a particular nanotube thus depends sensitively upon its chirality.

As the bandgap of a semiconducting tube arises from the quantization of $\vec{k_\perp}$, it is straightforward to show that the gap varies inversely with d. Further, projection of $\vec{k}$ into the Brillouin zone for a nanotube of arbitrary chirality (n, m) yields a condition for determining the electrical properties of that tube; all tubes satisfying the condition

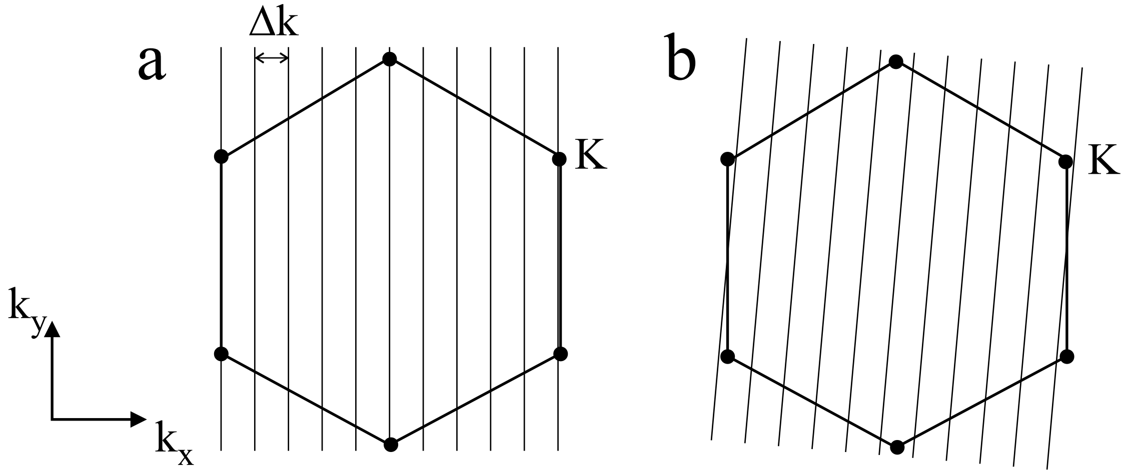

Figure 2.3: Allowed $\vec{k}$ after imposing periodic boundary conditions for (5, 5) and (6, 4) tubes. Adapted from [123]

$(n - m) = 3p$, where p is an integer, are metallic while all others are semiconducting. Accordingly all armchair tubes are metallic, while overall approximately two-thirds of tubes should be semiconducting. One should note that in addition to the bandgap induced by the imposition of periodic boundary conditions, a bandgap varying as $1/d^2$ may be induced in very thin metallic tubes due to curvature of the graphene sheet [88].

Near the Fermi level of a metallic nanotube the bandstructure may be approximated with a linear dispersion relationship, $E = \hbar v_F |\vec{k}|$, where $v_F \sim 8.1 \times 10^5$ m/s is the Fermi velocity [138]. This linearization of the nanotube bandstructure for low-energy excitations is standard in the literature.

For a more detailed description of the structural and electronic properties of carbon nanotubes, including detailed calculations of band structure for arbitrary chirality

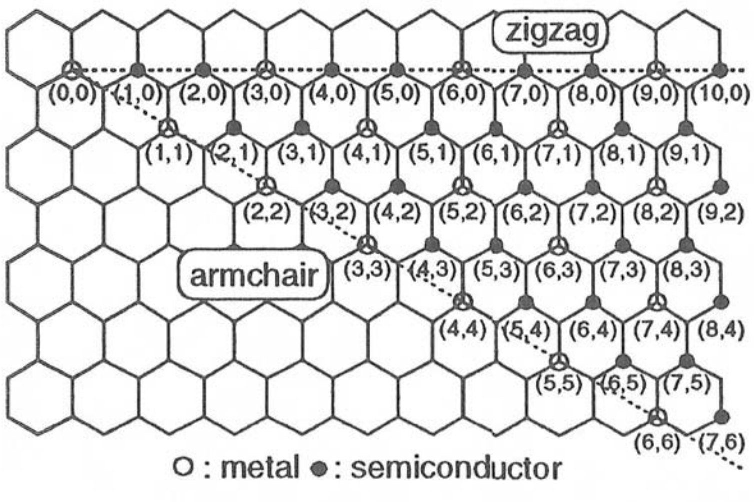

Figure 2.4: Nanotube type as a function of tube chirality (n, m).

the reader is invited to explore reference [138].

2.3 Chemical vapor deposition (CVD) growth of carbon nanotubes

While there are many nanotube growth techniques available, including arc discharge, laser ablation [65], and HiPCO, the work in this thesis will rely exclusively on a technique known as chemical vapor deposition, or CVD. The main distinction of this technique is that nanotubes are not grown in bulk, but are instead grown (with controllable density) *on-chip.* Thus, while those interested in mass production (kgs/day) would shy away from this technique [1], for researchers working with single tube devices, CVD is the nanotube growth method of choice.

The development of this technique followed a long-standing practice for the fab-

Figure 2.5: Nanotube CVD growth system built for nanotube synthesis using CH_4 as a carbon feedstock. At right are mass-flow controllers and an MKS multi-gas controller. At left is the Lindberg-Blue tube furnace, opened to reveal the quartz tube housing a quartz boat into which samples are loaded.

rication of vapor-grown carbon fibers [126], in which a gas phase carbon precursor is reacted in a high-temperature ($\sim$ 1000 C) furnace with a catalyst. We follow a recipe [90] originally developed at Stanford University by Jing Kong, in which methane is used as a carbon feedstock and nanotubes are grown from patterned catalyst islands.

Catalyst islands are patterned using standard electron-beam lithography techniques, and metallized with $\sim$ 0.7–1.1 nm of 4N purity Fe, deposited by thermal evaporation. (Alternative approaches involve the use of $FeNO_3$ nanoparticles, but all of the work presented in this thesis uses Fe as a catalyst). Immediately following liftoff in acetone and an isopropanol rinse, the chip is placed in a quartz boat and loaded into the CVD system. Further, it is oriented such that gas flow is perpendicular to the long axis of the catalyst island array (see Fig. 2.6a). In addition, an unpatterned chip coated with either Fe or $FeNO_3$ catalyst nanoparticles is loaded in the boat upstream from the target chip. The growth recipe follows: 1) 5.0 slm Ar purge at RT; 2)0.8 slm Ar + 0.1 slm H_2, heating RT→900 C over 30 m; 3)0.1 slm H_2 + 1.5 slm CH_4, 900 C for 15 m; 4) 0.75 slm Ar 900 C→RT over $\sim$ 2 h.

Nanotubes may subsequently be imaged and/or mapped relative to alignment markers through the use of an atomic force microscope (AFM). Single tubes typically range from $\sim$ 1–5 nm in diameter. Ropes of nanotubes are also typically present after growth, clearly identifiable by both large diameters and branching geometries.

Using transmission electron microscopy (TEM), we are able to identify single tubes with diameters less than $\sim$4–5 nm. Such tubes exhibit no visible internal structure, but do show a clearly defined outer wall. In contrast, ropes show considerable internal structure and often branching geometries, consistent with AFM analysis (Fig. 2.6b). We are therefore able to select single-walled nanotubes through AFM height and geometry analyses.

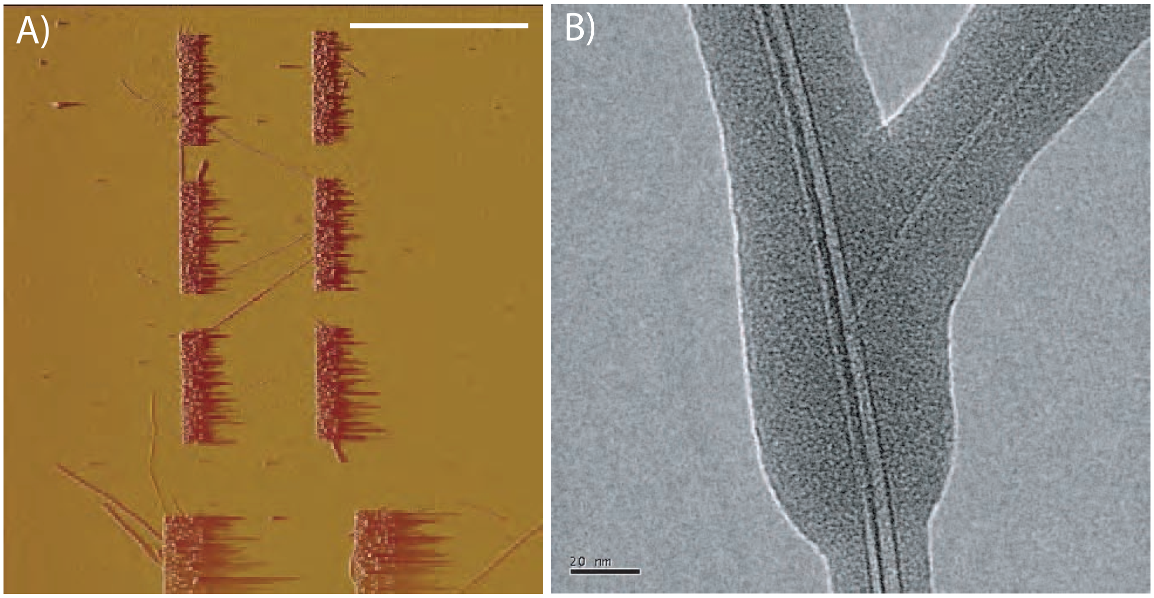

Figure 2.6: A) Carbon nanotubes grown from Fe catalyst islands in an AFM topographical image. Scale bar = 10 μm. B) TEM image of nanotubes grown across a slit in a Si3N4 membrane under standard growth conditions. A central rope with significant internal structure is visible with a single-walled tube branching off to the upper right of the image. Amorphous carbon deposited during TEM imaging is visible around the tube.

Chapter 3

Local gating of carbon nanotubes

In the field of condensed-matter physics, one ubiquitous technique for probing the electronic structure of a material or the interactions of charge carriers within it, is the measurement of transport through a device consisting of a piece of the material contacted by metal leads. For one disdainful of the field, a common insult slung at condensed-matter experimentalists is that we measure resistance for a living. In fact, this is not far from reality, but the amount of information accessible via transport is truly staggering; one needs only examine reference [17] to fully appreciate this. All of the material discussed in that now-famous review article relates to semiconductor heterostructures, but the field of carbon nanotube research has developed in a similar manner.

Shortly after the discovery of carbon nanotubes and subsequent theoretical treatments of their electronic properties, a number of research groups became involved in the study of electron transport in carbon nanotube devices. At the time of writing, an ISI publication search for “carbon AND nanotube AND transport” yielded 872 publications, while “carbon AND nanotube AND electronic” yielded 1292. I will not perform a historical overview of the field, but will instead insert references to previous work as appropriate in later sections of this thesis. For the interested reader, significant background material on the history of carbon nanotube electronic devices can be found in references [138, 2].

3.1 Fabrication of 2-terminal carbon nanotube devices

Carbon nanotubes are grown as described in section 2.3 from Fe catalyst islands patterned on an n^{++} As doped Si wafer with resistivity $\rho < 5$ mΩ-cm. This material is degenerately doped and hence conducting at all temperatures. The Si wafer was capped with a thermally grown layer of insulating SiO_2, typically 1 μm thick. Both the Si and SiO_2 emerge from the CVD growth process unaltered, with surface roughness comparable to to that measured prior to nanotube growth. By contrast, attempts to grow nanotubes on bulk GaAs or thin film Al_2O_3 deposited via atomic layer deposition largely failed due to a significant increase in surface roughness.

After growth, atomic force microscopy is used to locate nanotubes relative to the catalyst islands (see section 2.6). The catalyst islands are in turn aligned to both coarse and fine ebeam alignment markers patterned prior to tube growth. The AFM images are then imported into a CAD program after distortion from AFM imaging is subtracted. The images are fitted to the CAD drawing used in previous steps to pattern the catalyst islands relative to alignment markers. Using this procedure ebeam contacts are aligned to single-walled nanotubes selected for location, length, and diameter. In all cases contacts are designed in order to produce two-terminal devices. Such devices are limited by contact resistances, but there have not, to date, been successful four-terminal measurements on individual single-walled nanotubes. Contacts are then patterned and metallized, and subsequently an outer contact layer is aligned to these via optical lithography. The contacting material chosen has a significant impact on device performance and characteristics as will be discussed in the following two sub-subsections.

3.1.1 Tunnel contacts

Due to its chemical stability and ease of deposition and patterning, gold is the material of choice for the fabrication of nanoscale electronic wires for applications in cryogenic transport measurements. Gold, however, sticks poorly to most semiconductor substrates, and accordingly a wetting layer metal is generally deposited underneath the Au layer. This is typically Cr or Ti, either of which can be deposited via thermal evaporation using a standard W boat. The use of these metals in the fabrication of surface gates for semiconductor heterostructures carried over into the much younger field of carbon nanotube electronics, but brought with it a serious complication. The workfunction of Ti is 4.3 eV and that of graphite is ~ 4.5. Considering that the bandgap of a nanotube is of order 1 eV, and that most nanotubes are p-doped by ambient oxygen or water [10], using Ti as a contact material generally results in the formation of a Schottky barrier [74]. At cryogenic temperatures transport through such devices demonstrate characteristics linked to electron tunneling across a barrier as described in chapter 4.

3.1.2 Ohmic contacts

Considerable research investments were made worldwide in search of a technique to fabricate high-transparency contacts to carbon nanotubes. Early work demonstrated this ability using Au [102] without a Cr or Ti wetting layer, but device fabrication was complicated by poor adhesion and mechanical stability. Following this work, there were a number of papers published by IBM on transparent TiC contacts formed by annealing Ti contacts. However, total device resistance remained in the MΩ range, considerably higher than the ideal value of $\sim 6k\Omega$ for a single 1D subband (for a further discussion see section 9.1). Further, we were unable to successfully produce low-resistance contacts to nanotubes via annealing of Ti contacts. All of the experiments described in this thesis involving the use of ohmic contacts follow a 2003 paper [81] which detailed the use of Pd to produce transparent (non-Schottky) contacts to nanotubes (the workfunction of Pd=5.1 eV, nearly aligning it with the Fermi level of a nanotube which is doped into the valence band). Although following the contact recipe as prescribed in that text was never successful for us, we find that evaporating $\sim$ 15 nm of Pd typically yields devices with resistance of order 10–50 kΩ.

3.2 Local gating techniques

Considerable effort has focused on incorporating single-walled carbon nanotubes (SWNTs) into nanoscale analogs of solid-state electronic devices. SWNT transistors have been realized [147, 110, 167], as have nanotube circuits exhibiting more subtle features such as Coulomb charging and the Kondo effect [125, 146, 25]. In order to fully explore the richness of nanotube device physics, independent control of relevant physical parameters is required. Many of these may be controlled by electrostatic gating, in which the SWNT device is capacitively coupled to one or more nearby gate voltages.

There have been a number of recent advances in gating of SWNT devices, including the use of Al backgates with thin oxide layers [11, 144], the use of high-k dielectrics [82], metallic side gates [80], liquid-phase electrolyte solutions [137], and external scanned gates [56, 26, 145]. However, a technique for implementing local gating via standard lithography in devices utilizing chemical vapor deposition (CVD) nanotube growth had not yet been presented at the time our experiments commenced. In previous work, nanotube devices with multiple electrostatic topgates [82] or a metallic gate underneath the nanotube [83] were fabricated to produce multigate devices, including OR logic transistors. In these cases, however, data appeared consistent with a global coupling of all topgates. More recently, experimental work has also indicated that it is possible to gate spatially localized sections of a nanotube device [166]. This work focused specifically on gate control over room-temperature SWNT-based field effect transistors fabricated using random nanotube deposition, however.

In this section I will describe the several techniques we have employed in order to achieve local gating of carbon nanotubes.

3.2.1 Undergating

Introduction

In this section we report a technique for achieving local control of CVD-grown nanotube conduction via multiple electrostatic gates. Device fabrication is based on growth of SWNTs from Fe catalyst, and takes advantage of two notable processing features: (1) Thin Mo ”finger gates” (150 nm wide), robust against the CVD process, are defined lithographically, allowing nanotubes to be grown across them. (2) A high-k dielectric layer is patterned by photolithography and a liftoff procedure using low-temperature atomic layer deposition (ALD) [23]. Transport data (see B) from a nanotube device fabricated in this manner indicate that the effect of individual finger gates is qualitatively different from that of a global backgate.

Device fabrication

Devices were fabricated on doped Si wafers with 1 mm of thermally grown oxide as a base substrate, allowing the conducting Si to be used as a global backgate. Before nanotube growth, sets of five parallel Mo finger gates roughly 150 nm wide and ¡ 10 nm thick, spaced by ∼400 nm, extending approximately 100 mm in length (Fig. 3.1), were patterned using electron-beam lithography liftoff and deposited using electron-beam evaporation. Larger Mo lines connected to the fine Mo gates were then patterned with photolithography liftoff.

Mo was chosen for its tolerance to the high temperatures and reducing atmosphere used in CVD processing, combined with reasonably low resistivity in thin-film form. Similar conclusions favoring Mo for this purpose were reached independently in Ref.

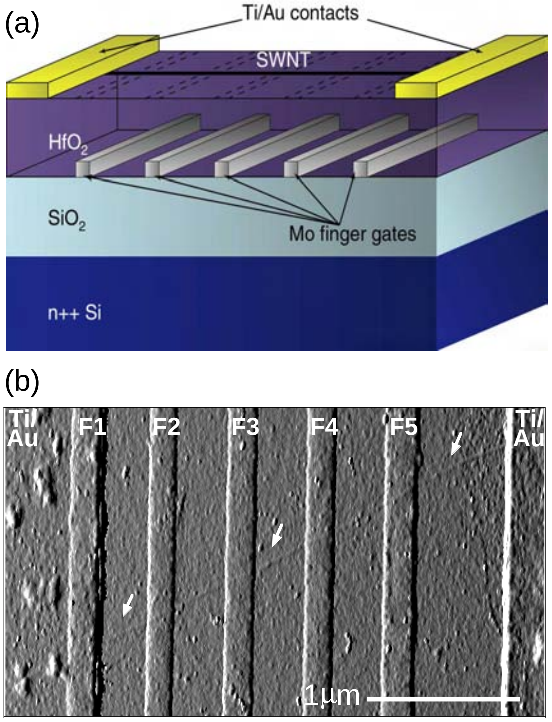

Figure 3.1: a) Schematic of finger gated devices. Mo gates (150 nm wide 10 nm thick) were defined lithographically on a Si/SiO$_2$ substrate and subsequently coated with 25 nm of HfO$_2$ grown by low-temperature ALD. Nanotubes were grown across these local gates by CVD and contacted with Ti/Au electrodes. Not to scale. b) Atomic force micrograph of nanotubes grown across Mo finger gates and contacted (far left and far right) by Ti/Au leads. Note one finger gate passes directly underneath the nanotube-metal contact. Arrows indicate the location of the nanotube. Finger gates are labeled as in the text.

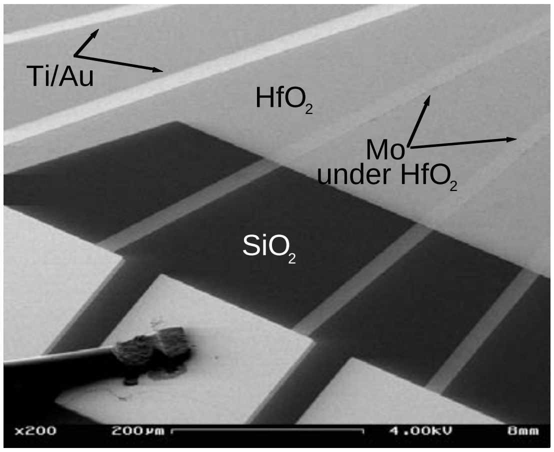

Figure 3.2: Scanning electron micrograph showing liftoff-patterned ALD oxide mesa edge (middle) showing Ti/Au wires on top of the mesa (upper left) and Mo wires running underneath the patterned ALD (bottom)

[55]. Thin gate metallization (<10 nm thickness) was used to avoid bending defects created by a nanotube "draping" over raised contacts [18]. We found that 5 nm films of Mo exposed to CVD processing vanished, while thicker layers remained intact (minus ~5 nm). Thus, metal which was exposed to the CVD environment always included a ~5 nm sacrificial layer.

After fabrication, the finger gates and their connections were covered by 25 nm of HfO_2, deposited using low-temperature ALD and patterned using photolithography and liftoff [23]. The dielectric layer was patterned to form large mesas that covered the finger gates but left the contacts exposed, as shown in Fig. 3.2. Next, rectangular patterns ($\sim 1mm \times 5mm$) were defined in a poly(methyl methacrylate) (PMMA) layer using electron-beam lithography, and ~1 nm Fe was deposited using thermal evaporation. The rectangles were oriented in rows on either side of the Mo finger gates, and served to locate the Fe catalyst to promote nanotube growth across the underlying finger gates. A standard CVD recipe using methane as a carbon source was employed for tube growth (see section 2.3), after which SWNTs crossing the finger gates were located using an atomic force microscope (AFM). Finally, SWNTs were contacted with Ti/Au contact pads to complete the devices (Fig. 3.1b). Typical device dimensions (between contacts) were 3 – 5mm. Atomic force and (post-measurement) scanning electron microcopy ensured that the finger gates were continuous.

Unfortunately, this fabrication technique proved quite difficult, and transport measurements (Appendix B) did not clearly demonstrate the ability to locally deplete carriers in multiple sections of a single nanotube. As such, this gating method was eventually abandoned for alternative approaches described in the following subsections.

3.2.2 Sidegating

An alternative approach employed for the fabrication of spatially localized electrostatic gates along the length of a nanotube requires lateral alignment of gate electrodes in close proximity to the tube. Gates are aligned to nanotubes in a manner similar to that in which contacts are aligned. Alignment error of order 100 nm intrinsic to AFM imaging on our Veeco multimode system makes lateral alignment somewhat irreproducible.

Measurements have shown that in order to apply a spatially localized voltage, sidegates must be within 100 nm of a nanotube. A common failure mode for these devices involved poor alignment resulting in nanotubes shorted to gate electrodes. Due to these difficulties this technique is used only occasionally, but was utilized in the acquisition of the data presented in section 9.2. A representative device is shown

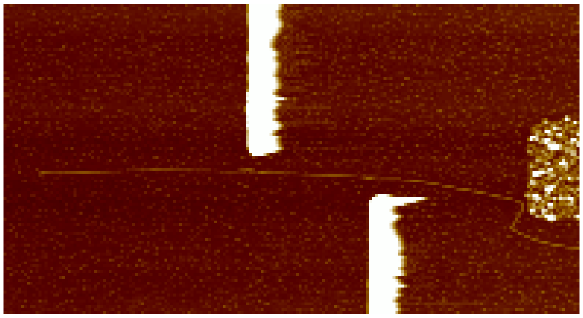

Figure 3.3: AFM height image of a carbon nanotube with laterally aligned sidegates.

in Figure 3.3.

3.2.3 Topgating

By far the most successful technique in locally gating nanotubes has involved a topgating geometry in which nanotubes were embedded in an insulating layer, and electrostatic gates aligned over the nanotube devices. Here I will briefly describe the techniques developed and employed in our lab.

Top-gating was demonstrated successfully by two groups prior to our adoption of the technique [167, 82]. In our lab, considerable effort went into the formulation of a recipe which did not damage nanotubes or lithographically patterned electrodes, and also produced thin-films of sufficient quality to minimize gate leakage. Initial successes came with the use of an electron-cyclotron resonance (ECR) plasma-enhanced chemical vapor deposition (PECVD) system to deposit SiO_2. Standard recipes for oxide deposition, however, required the use of highly energetic plasmas (microwave power in excess of 500W) during deposition, which destroyed nanotube devices. A new recipe utilizing both low microwave power and a high process pressure (in order to reduce plasma mean free path) was developed to address these problems without sacrificing oxide film quality. Etch tests, SEM analysis, and electrical characterization showed that films with thickness $\sim$ 20–30 nm were similar in quality to thermally grown oxide. The recipe follows:

PECVD recipe: *Purge:* 25 sccm (standard cubic centimeters per minute) Ar at P = 7 mTorr, 30 s. *Equilibrate:* 10 sccm Ar + 20 sccm O_2 + 50 sccm SiH_4 (3%) at P = 100 mTorr, 60 s. *Deposit:* 10 sccm Ar + 20 sccm O_2 + 50 sccm SiH_4 (3%) at P = 100 mTorr, 50W microwave, 90–120 s.

For reasons described in subsequent experimental sections, we eventually abandoned the use of PECVD grown SiO_2, and moved to an alternative deposition technique called atomic layer deposition (ALD) [99]. Details of the atomic layer deposition process may be found in Appendix A, but the recipe used for the fabrication of nanotube devices coated with $\sim$ 35 nm of Al_2O_3 is presented below, and a representative ALD system is depicted in Figure 3.4.

ALD recipe: *Substrate Temperature:* 120 C. *Valve Temperature:* 70 C. *Pump:* 20 min at P $\sim 10^{-2}$ Torr. *Pulse 1:* 15 ms H_2O. *Exposure:* 15 s wait. *Pump:* 15 s. *Pulse 2:* 15 ms TMA. *Exposure:* 15 s wait. Repeat starting with Pulse 1, 350 cycles.

After dielectric deposition, gate electrodes are patterned via ebeam lithography such that a series of gates crosses a single tube. Gate widths and configurations vary by experiment, but most are $\sim$ 150 nm across, and $\sim$ 50 nm thick. Top-gates were generally connected to on-chip voltage buses such that multiple devices were addressed by a single dc connection. After optical contacting of the ebeam pattern, this technique facilitated the fabrication of $\sim$10 nanotube devices per chip, each with 3–5 topgates, without the necessity of 30–50 individual connections to cryostat wiring.

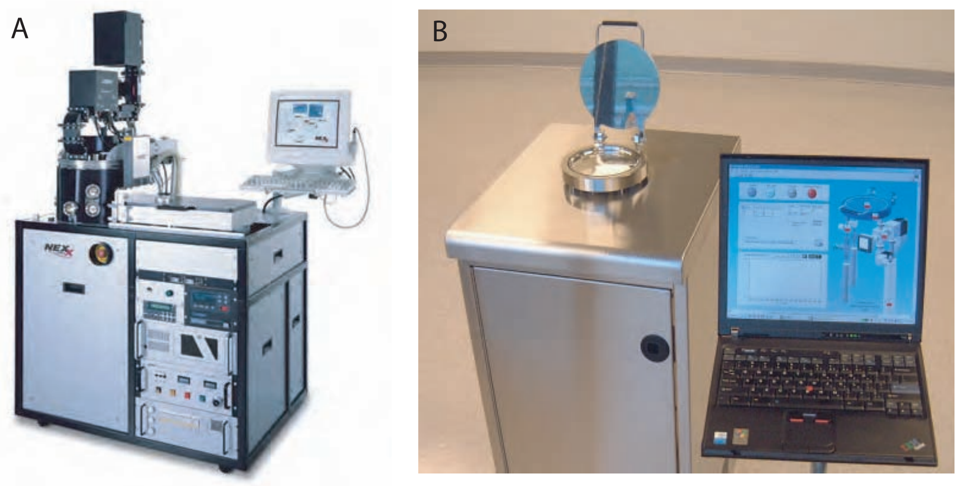

Figure 3.4: A) Image of NEXX Cirrus PECVD system B) Cambridge Nanotech ALD system. Both images are similar to actual systems used.

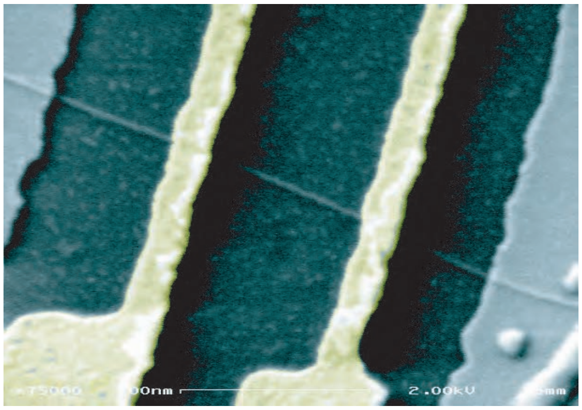

Figure 3.5: False-color SEM image of a carbon nanotube contacted with metal electrodes under an insulating dielectric layer. Electrostatic top-gates aligned to the device are highlighted in yellow.

A representative top-gated device is shown in Figure 3.5.

Chapter 4

Single electron charging

Electron transport diverges radically from Ohm's law in small conductors measured at sufficiently low temperatures. Generally, when a conductor is coupled to leads via a tunnel junction (a classical energy barrier through which electrons may be transported via quantum mechanical tunneling), a well-defined electrostatic energy is required to move charge across a barrier. A double tunnel junction with a central island and capacitively and resistively coupled leads is often referred to as a single electron transistor or a quantum dot. In this chapter I will detail some of the relevant properties of quantum dots, and describe the transport characteristics which we measure in the lab. For a more detailed discussion of single electron charging, the interested reader is referred to Ref. [94].

4.1 Single electron tunneling and the Coulomb blockade

The phenomenon of single electron tunneling arises from classical electrostatics, but results from quantization of charge in units of e. It is therefore not straightforward to claim that it is a purely classical or quantum mechanical effect. Here I will outline some of the basic characteristics of single electron tunneling.

4.1.1 The single electron transistor

Figure 4.1a represents a simple equivalent circuit for a single electron transistor (SET), or quantum dot: an island coupled capacitively and resistively to electron reservoirs. In addition, a capacitively coupled gate voltage, V_g, which shifts the electrochemical potential of the island linearly with applied voltage may be present, but largely will be ignored in this section. The material from which the single electron transistor is fabricated can vary from laterally and vertically defined quantum dots in semiconductor heterostructures [93], to carbon nanotubes, to small metal grains [134]. The basic phenomena observed in these diverse structures are all identical, and linked (as their names imply) to the addition of single electrons to the island. It is worthy of note that single electron tunneling, also known phenomenologically as Coulomb blockade, can occur in any tunnel junction. Our discussion will focus exclusively on the quantum dot, however.

The first energy scale relevant to single electron charging is derived from the classical energy to charge a capacitor. The requirement that an electron have sufficient energy to overcome this energy barrier to tunnel onto the island results in the now famous Coulomb blockade of transport which will be discussed in the following section of this chapter. In this case, the charge added to the capacitor (the island) is a single electron of charge e, yielding a classical charging energy, $E_C = e^2/C_\Sigma$, where $C_\Sigma = C_L + C_R + C_G$ is the total capacitance of the island. Phenomena associated with this energy scale will only be visible when temperature is the lesser energy. The dimensions of a typical single electron transistor are of order microns or nanometers, producing total island capacitances $\sim$ aF. Thus, in order to satisfy the relation $E_C > k_B T$, measurements temperatures must be of order mK–K, requiring cryogenic systems. C increases with increased island size, and hence the requisite measurement T decreases. Modern dilution refrigerators are capable of cooling to 5–10 mK, thus placing a limit on the absolute size of the SET to be measured.

In addition to the classical charging energy there is an additional energy scale in the problem of single charge tunneling, namely the mean level spacing, Δ. This is the energy level separation arising from quantum confinement of electrons to the island. In a simple particle-in-a-box picture, it is the discrete energy level spacing between allowed modes in a quantum mechanical treatment. Coulomb blockade may be observed in systems in the *classical* regime where $\Delta < k_B T$, so long as the the charging energy dominates temperature. The influence of the mean level spacing will become apparent in the following section.

In order to observe single electron charging, it is necessary that quantum mechanical fluctuations of charge (δe) across the tunnel barriers isolating the SET from its leads be less than $|e|$, hence a charge on the island will be well localized if $\delta e < E_C$.

This imposes a constraint on the resistance of the tunnel barriers. From the uncertainly principle we know that $\delta e = \hbar/\tau_{RC}$ where $\tau_{RC} = R_i C_\Sigma = C_\Sigma/G_i$ is the time constant associated with charging the island across barrier i. Replacing E_C with its definition above we find a constraint on the barrier conductance, $G_i < 2e^2/h$. A similar result may be reached through a quantum mechanical treatment of tunneling across a barrier [41]. Note that $2e^2/h$ is also the spin degenerate quantum of conductance (See section 9.1). Hence, junction resistance must be $> h/2e^2$ in order to sufficiently suppress extended state wavefunctions and produce an electron localized on the island.

4.1.2 Transport properties of quantum dots

For the circuit diagram shown in Figure 4.1a, it is possible to determine the transport characteristics of a quantum dot exclusively using classical electrostatics, considering the addition of a single charge to a capacitor (for a thorough investigation of this problem see Reference [32]). Instead, I will primarily approach this problem from the single particle energy level perspective.

The Coulomb gap

I have already introduced the classical charging energy, E_C required to add an electron to a quantum dot. The most prevalent manifestation of this energy gap between allowed single particle levels appears in the IV curve for a quantum dot. As a function of applied voltage bias, V_{SD}, conductance is suppressed for $|V_{SD}| < |e/2C|$, the Coulomb gap. Alternatively this may be expressed by saying that conductance

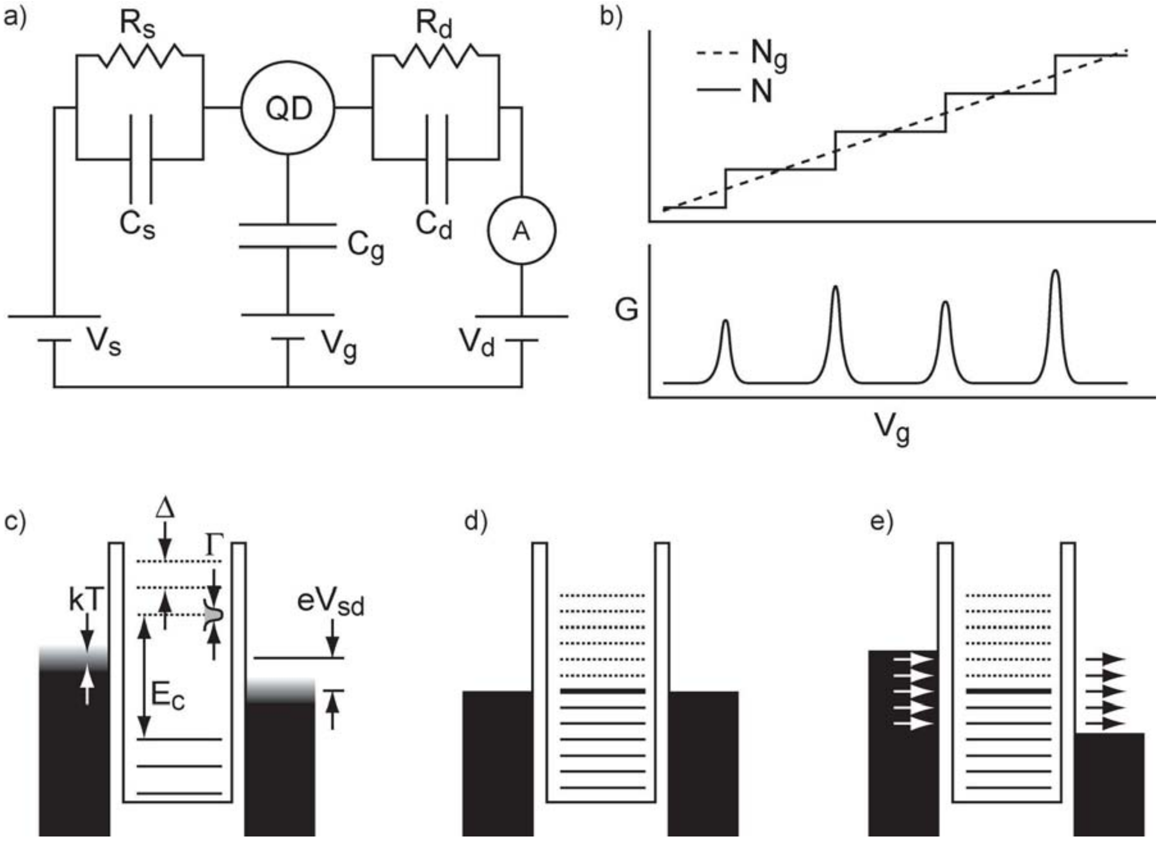

Figure 4.1: a) Circuit diagram for a quantum dot resistively and capacitively coupled to source and drain electrodes. A gate voltage is also capacitively coupled to the dot. b - upper panel) induced charge on the quantum dot as a function of gate voltage. The dotted line is the continuous gate charge while the solid line is the actual charge on the island. b - lower panel) Conductance as a function of gate voltage showing Coulomb blockade peaks at the degeneracy points between discrete charge numbers on the island. c) Schematic level diagram for a quantum dot showing the charging energy, E_C, the effect of temperature and lifetime broadening. d) Zero-bias condition of ground state alignment of the dot chemical potential with that of the leads. Single particle levels spaced by Δ are represented. e) Finite bias condition illustrating allowed transport through multiple levels in the dot. Figure adapted from [84].

is suppressed until a virtual charge of $e/2$ is induced on the dot by V_{SD} across C_S, overcoming the Coulomb gap and permitting a charge to tunnel onto the island.

In the zero-bias case it is also possible to induce a charge on the quantum dot via the capacitively coupled gate voltage. The upper panel of Fig. 4.1b shows the continuous gate charge (dotted line) induced on the island $N_g = C_g V_g$. As mentioned above, however, charge is quantized in units of e, and as such the island charge cannot change continuously. Instead it changes in a stepwise manner, with each charge added when the induced gate charge $N_g = e/2$. At this degeneracy point current flow through the quantum dot is permitted, producing a peak in conductance (Fig. 4.1b, lower panel) whose lineshape is determined as described below. In the single particle picture (Fig. 4.1d), this occurs when an energy level of the dot is aligned with the Fermi level of the leads. As such, one may consider the gate voltage to shift the bottom of the energy band in the quantum dot, moving energy levels into and out of alignment with the source and drain chemical potentials. When the band has been moved by E_C, a single particle state becomes accessible, a single electron is added to the dot and current is allowed to flow. The charging energy is a Fermi surface property of the quantum dot, i.e. occupied energy levels are not spaced by E_C, but only Δ (Fig. 4.1c, d). Thus the charging energy is often included only in discussion of the *addition energy* of an electron to the dot.

Coulomb blockade peak shape

The rate of tunneling across the barriers defining the dot, Γ, depends upon the physical characteristics of the barriers. In addition Γ is also used to denote the FWHM linewidth of the Coulomb blockade peaks for the case of resonant tunneling. One may show that the lineshape of a single particle energy level is given by the Lorentzian [41]

$$T(E) = \left(\frac{\Gamma_1\Gamma_2}{\Gamma_1+\Gamma_2}\right)\frac{\Gamma_1+\Gamma_2}{(E-E_R)^2+((\Gamma_1+\Gamma_2)/2)^2}. \tag{4.1}$$

where the subscripts $1, 2$ denote the two tunnel barriers defining the dot. Physically, one may envision this as a broadening of the energy level due to the uncertainty principle: the electron has a finite lifetime in the dot set by the tunnel rates into and out of the dot which requires energy uncertainty.

In practice, however, the dominant lineshape of a Coulomb blockade peak is derived from thermal broadening of the Fermi seas in the source and drain leads. Finite temperature produces a smearing of the Fermi function with approximate width k_BT around the Fermi Energy (Fig. 4.1c), and accordingly transport will be allowed when the energy level of the dot is aligned within this energy window. We know that the current through a state may be written [41]

$$I = \int i(E)\, dE \tag{4.2}$$

$$i(E) = \frac{2e}{h}\overline{T}(E)[f_1(E) - f_2(E)] \tag{4.3}$$

where $\overline{T}(E)$ is the transmission function through a 1D mode and $f(E)$ is the Fermi function. Here the subscripts refer to the reservoirs on either side of a tunnel barrier. In the linear response we may write

$$\delta I = \frac{2e}{h}\int \Big(\overline{T}_{eq}(E)\delta(f_1 - f_2) + (f_1 - f_2)\delta\overline{T}_{eq}(E)\Big) \tag{4.4}$$

$$\delta(f_1 - f_2) = -\left(\frac{\partial f_0}{\partial E}\right)[\mu_1 - \mu_2] \tag{4.5}$$

where μ_i is the Fermi level of conductor i. Thermal smearing of the Fermi sea enters through the term

$$F_T(E) = -\left(\frac{\partial f_0}{\partial E}\right) = \frac{1}{4k_BT}\cosh^{-2}\left(\frac{E}{2k_BT}\right). \tag{4.6}$$

Thus the lineshape of a thermally broadened Coulomb blockade peak has the form $\cosh^{-2}(E/T)$. The numerical factors in this form vary slightly depending upon the relative values of the relevant energy scales. For the case $\Gamma < k_BT < \Delta, E_C$, the width of the peak in energy, $\Delta E^{FWHM} = 3.5k_BT$, while in the case of *classical* Coulomb blockade where $\Gamma < \Delta < k_BT < E_C$, and many single particle levels participate in transport, $\Delta E^{FWHM} \approx 4.4k_BT$. In both cases, however, peak conductance scales as $1/T$ while peak width scales as T.

Application of a finite dc bias

Between Coulomb blockade peaks the dot conductance is suppressed as there are no available single particle level at the lead chemical potentials. At zero bias one thus sits in a "Coulomb valley" with fixed electron number on the dot (lower panel, Fig. 4.1b). If the dc bias, V_{SD}, across the dot is increased sufficiently, an unoccupied state above the zero-bias lead chemical potentials will now fall in the bias window, and become accessible to transport (Fig. 4.1c). For a fixed drain voltage, shifting V_{SD} implies applying a voltage to the source electrode, increasing its chemical potential linearly with V_{SD}. Similarly the bottom of the dot energy band (and hence any single particle level) shifts linearly with applied V_g. Thus, in order to access a state which has been shifted in energy by eV_g, one must apply $V_{SD} = \alpha^{-1}V_g$ in order to lift the Coulomb blockade, where $\alpha^{-1}e$ is the conversion factor between gate voltage and energy. This phenomenon is symmetric in the sign of V_{SD}. If one plots current as a function of both V_{SD} and V_g, Coulomb blockade peaks evolve as straight lines away from the $V_{SD} = 0$ line. Completing this plot leads to the formation of Coulomb diamonds, outside of which current flow is allowed. Like the $V_{SD} = 0$ Coulomb valleys, charge number is fixed on the dot inside the finite bias diamonds.

The application of a finite V_{SD} across the dot also allows multiple quantum levels of the dot to be occupied (Fig. 4.1e). Thus transport measurements often reveal a *Coulomb staircase* in the *IV* curve of a quantum dot: a step in current is observed each time another quantum level is accessed (there are additional requirements on relative tunnel barrier strengths, see Ref. [70]).

(It is worthy of note that in the electrostatics derivation of single electron tunneling across a tunnel junction, the nature of the bias across the junction determines whether or not Coulomb blockade is observable. The application of a voltage bias across a junction, through the simple relationship $Q = CV$ dictates that the tunnel junction resistance, R_T, will produce an ohmic response. This results because a fixed voltage bias implies a fixed charge on the capacitor. Any charge that tunnels is instantly compensated by the voltage bias, and the current through the junction is given simply by V/R_T. If instead the junction is current biased, the current source continuously charges the capacitor, and the finite R_T allows single charge tunneling. In this case, energetic considerations related to the charging/discharging of a capacitor dictate the *IV* curve, producing a Coulomb gap. In a quantum dot, under a voltage bias, the first junction may be considered a current source, thus single electron tunneling characteristics are observable.)

Influence of electron spin

The Pauli exclusion principle states that no two electrons may exist in the same quantum state. Thus, only two electrons may be added to any discrete state in a quantum dot, each with opposite spin quantum numbers. In the simplest case of noninteracting electrons, this influences the spacing of Coulomb blockade peaks in a quantum dot (in the *quantum* Coulomb blockade regime) by adding the requirement that every other electron be added to a new quantum level. Thus, starting with zero electrons one may add an electron of e.g. spin up for a cost of E_C. The next electron may be added to the same quantum state with opposite spin for E_C. Adding the third electron, however, requires accessing the next available quantum level. Thus an energy, $E_C + \Delta$ is required, followed by an electron with E_C, the next at $E_C + \Delta$ and so forth. Accordingly, Coulomb blockade peaks are spaced by alternately small and large gate voltages, corresponding respectively to single particle spacings of E_C and $E_C + \Delta$. This is often referred to as even-odd filling, and combined with magnetic field spectroscopy of energy levels, is a clear indication of spin physics in quantum dots. In the presence of a magnetic field each two-fold degenerate state splits into its two spin-polarized components due to the Zeeman energy $E_B = \sigma g \mu_B B$ where $\sigma = \pm 1/2$ is the electron spin, μ_B is the Bohr magneton and B the magnitude of the applied field.

4.2 Measurement of Coulomb blockade in single quantum dots

4.2.1 2-wire voltage bias configuration

Coulomb blockade is generally measured at $V_{SD} = 0$ where the source and drain chemical potentials are aligned. As the Coulomb blockade is a manifestation of a nonlinear IV response, it is necessary to probe the low-bias subspace in order to observe blockade peaks. This is generally accomplished in one of two ways; the linear response regime may be probed directly by exciting the system with a small oscillating voltage, or the nonlinear dc IV curve may be measured and numerically differentiated. In either case, the measurement provides information about the *differential conductance*, dI/dV, of the system.

Typically, dI/dV is measured using a lock-in amplifier; the lock-in outputs an oscillating voltage bias which is applied to the device (after division) and the output current is measured. In a cryogenic system it is necessary that the ac excitation $V_{ac} < k_B T$ such that the *effective* electron temperature induced by the oscillating potential does not mask the physical phenomena one is looking to explore. Using the conversion 1 K $\sim$ 86 μV, one must generally use $V_{ac} \sim 10$ μV in either a ^{3}He or dilution refrigerator. In our lab it is standard practice to feed the output current into a current preamplifier which converts the current into a voltage with a user-defined ratio. The resulting voltage, oscillating at the source frequency, is then fed back into the lock-in amplifier and mixed with a reference signal at the same frequency, yielding dc and $2f$ outputs (the $2f$ component is filtered out).

Alternatively, one may simply source a dc bias across the device, using, for example, a digital-analog converter (DAC) or another voltage source such as a source-measure unit. Again, the sourced voltage is generally divided down before being applied to the sample, and the resulting dc current is measured as above. This has the advantage of allowing faster data collection than ac measurements, as sweeping the dc V_{SD} may introduce harmonics of V_{AC} which can overload a lock-in and require a wait time at each point in a scan. A dc measurement, however, does not benefit from the noise filtering capabilities of the phase sensitive detector which forms the basis of the lock-in amplifier, and considerable pickup in a measurement may make numerical data differentiation difficult or impossible.

A *4-wire* configuration is often used to measure devices in which the device resistance may be smaller than other series resistances. In quantum dots, however, the total measured reistance is generally dominated by the tunnel barriers (exactly what we wish to measure) and hence this technique is not typically used. Further, as we will see in the next section it is quite difficult to fabricate a four-terminal device using a carbon nanotube.

4.2.2 Quantum dots based on carbon nanotubes

Coulomb blockade in carbon nanotubes was first studied in detail by Bockrath et. al [25] in 1997. In that study, and many others to follow, a quantum dot was formed from the section of a nanotube (either a rope or a single tube) between metallic contacts. The contacts formed tunnel barriers at the metal-nanotube interface and allowed the observation of single electron charging effects at low temperatures.

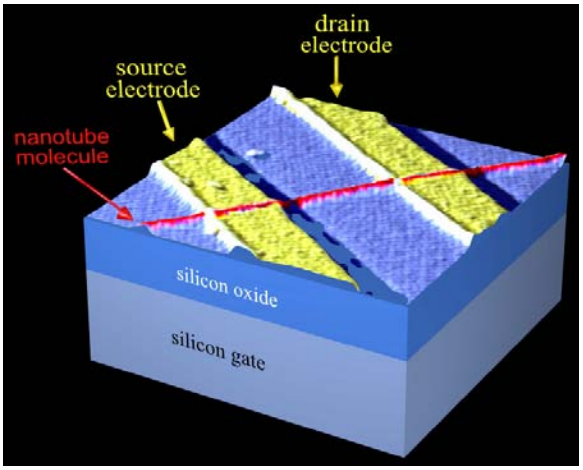

Figure 4.2: A carbon nanotube 2-terminal device operated as a quantum dot. Figure adapted from [43].

Tremendous research effort has been invested in studying carbon nanotube quantum dots [25, 26, 125, 103] with new results emerging to this day (e.g. Ref. [140]) from simple 2-terminal devices consisting of a nanotube contacted at source and drain and a capacitively coupled backgate electrode, usually the Si substrate of the device. Here I will provide a bit of background on carbon nanotube quantum dots, and in Chapter 7 I will introduce a new device geometry for the fabrication of gate-defined quantum dots along the length of a single nanotube, which does not rely upon tunnel barriers at the metal-nanotube interface.

In nanotube quantum dots, E_C is generally of order mV, and is set by the capacitance of the device. Approximating the capacitance per unit length from the formula for a coaxial cable $C/L = 2\pi\varepsilon\varepsilon_0/\ln(2h/r)$ where ε is the dielectric constant of SiO$_2$ $\sim$ 2.5, h the tube to backgate distance and $r \sim 1$ nm the tube radius, we find a capacitace per unit length, $C/L \sim 19$ aF/μm, and hence a charging energy, $E_C \sim 8$ meV/μm, for 1 μm gate oxide.

The zero-dimensional energy level splitting, Δ, may also be calculated for a carbon nanotube quantum dot of length L. In addition to the quantization of transverse momentum along the circumferential direction, the finite extent of a carbon nanotube quantum dot leads to quantization of momentum along the tube axis as $\Delta k = 2\pi/L$. Linearity of the bands near the Fermi level suggests that one may write

$$\Delta = \frac{\hbar v_F \Delta k}{2 \times 2} \tag{4.7}$$

which gives $\Delta \sim 0.8$ meV/μm. The factors of two account for the band and spin degeneracy of the 1D subbands, and may be omitted as appropriate for a particular device (e.g. band degeneracy is often lifted by strain).

Transport measurements on two-terminal nanotube devices with tunnel contacts show clear signatures of Coulomb blockade as shown in Fig. 4.3 [123]. Differential conductance measured as a function of gate voltage shows Coulomb blockade peaks which evolve with applied V_{SD} to form familiar Coulomb diamonds. Excited states are clearly visible outside of the diamonds, and state splitting in an applied magnetic field is also evident.

For contacts that are sufficiently transparent, additional features such as the Kondo effect [125] become visible (a full discussion of this feature is beyond the scope of this thesis and may be found in Ref. [123]). In addition, the four-fold degeneracy of the carbon nanotube band structure has been revealed in linear response Coulomb blockade measurements as in Fig. 4.4. Here, four electrons may be added to a single orbital level (spaced by E_C) due to the appearance of band and spin degeneracy in the tube. The spin filling of these orbitals and the effect of exchange coupling is examined thoroughly in Ref. [103]. Similar measurements derived from excited state

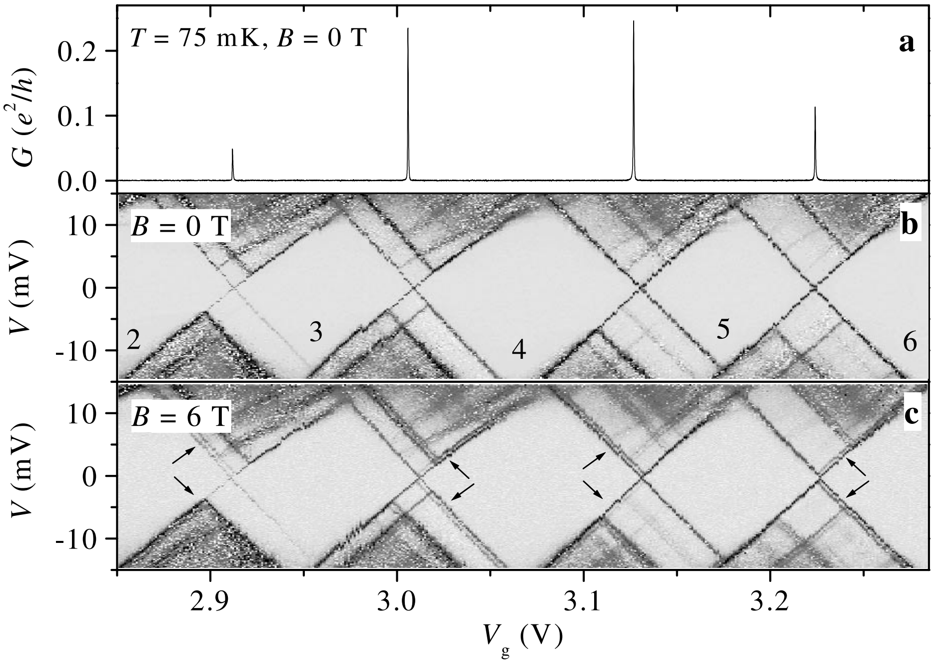

Figure 4.3: a) Conductance as a function of gate voltage showing Coulomb blockade peaks measured at $T = 75$ mK in a nanotube quantum dot. b) Bias spectroscopy reveals Coulomb diamonds with excited states visible. c) Measurement conducted at $B = 6$ T showing Zeeman splitting of electron states marked by arrows. Figure from [123].

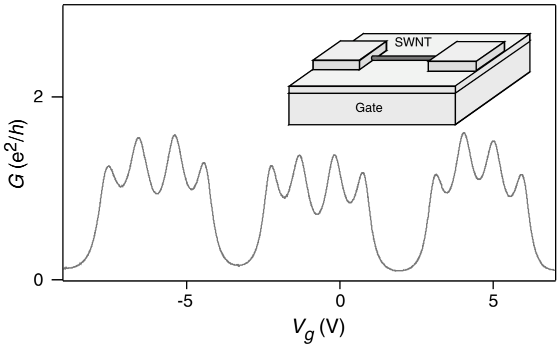

Figure 4.4: Coulomb blockade peaks for a tube ∼ 100 nm between contacts. Four-fold periodicity of the peaks is evident. Figure from [103].

spectroscopy have recently been reported in Ref. [140] as well.

4.3 Transport in double quantum dots

While considerable effort is still being focused on transport measurements of single quantum dots, there has been a shift in the community towards more complex systems. The motivation for this new focus is largely derived from a growing interest in demonstrating the formation and manipulation of coherent quantum states in a solid-state system. The incremental (and logical) extension of a single quantum dot is the double dot, whose transport characteristics are derived from the physics of single electron charging, similar to transport in single dots. Additional complexity enters the problem, however, due to the possible *interaction* between the two quantum dots. In this section I will describe the transport characteristics of series double quantum dots (Fig. 4.5), laying the groundwork for the experimental results presented in Ch. 5. Much of the material presented in this section is derived from reference [154], a review of transport experiments in double quantum dots.

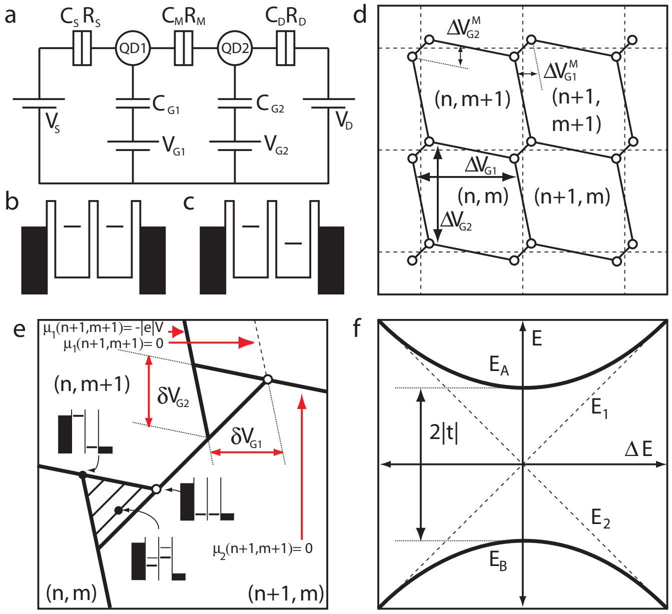

Figure 4.5: a) Circuit diagram for a series double quantum dot. b) Energy level diagram for resonant and c) nonresonant level alignment between dots. d) Schematic diagram of a double dot charge stability diagram. Dotted intersecting lines represent the positions of Coulomb blockade peaks as a function of two independent gate voltages in the absence of interactions between the dots. The electron number in both dots is well defined in each cell of the square pattern, and crossing a line represents the addition of an electron to one dot. The addition of a mutual capacitance, C_M, between the dots splits the intersection points into a pair of vertices (circles) known as triple-points (as they correspond to energy degeneracy between three charge configurations), and produces a honeycomb charge stability plot. In the case of a series double dot, the vertices correspond to resonant alignment of energy levels between the two dots and represent the only locations in gate-space where transport through real states is allowed. See text for a more detailed description of the honeycomb cell dimensions. e) The application of a finite dc V_{SD} causes the expansion of the triple-points into triangular regions defined by the magnitude of V_{SD}, and the extremal positions of the two dot chemical potentials within the bias window. The resonant alignment of excited states in the two dots produces a series of stripes within the finite bias triangles, and representative level diagrams show energy level alignments at various points on the charge stability diagram. f) The addition of tunnel coupling between the two dots also leads to a splitting of the charge degeneracy points due to the formation of symmetric and antisymmetric combinations of energy states. The magnitude of the splitting is given by the tunnel coupling strength. The axis E represents the total energy axis, diagonal bottom-left to top-right in the honeycomb diagram shown in panel d. ΔE is the dc detuning between the energy levels of the two dots. Parts after [154].

4.3.1 The charge stability diagram

In the absence of interactions between two quantum dots, each with an independent gate electrode (Fig. 4.5a), Coulomb blockade would occur in both dots independently (if it could be measured, for example in a parallel configuration where transport could be measured through each dot). In a two-dimensional plot of Coulomb blockade peak position as a function of both gate voltages (dotted lines, Fig. 4.5d) peaks would evolve to form a square grid. As the space between each line corresponds to a Coulomb valley for a single dot, the square grid defines regions of gate-space with well-defined charge number in both dots. Further, at the intersection points of these lines, energy levels in both dots are aligned with the Fermi levels of the leads (Fig. 4.5b), and transport is allowed. Along the edges of these squares, however, only a single dot's energy level is aligned with the leads (Fig. 4.5c), and transport through real states is forbidden.

The addition of a mutual capacitance between the dots shifts the charge stability diagram to the honeycomb pattern shown in Fig. 4.5d. Here, the addition of a charge e to dot 1 induces a charge on dot 2 by way of the capacitace C_M. Using a vector formalism for the relationship between charges, capacitances and energies [154], one may define a series of renormalized charging energies

$$E_{C1} = \frac{e^2}{C_1}\left(1 - \frac{C_M^2}{C_1 C_2}\right)^{-1} \quad E_{C2} = \frac{e^2}{C_2}\left(1 - \frac{C_M^2}{C_1 C_2}\right)^{-1} \quad E_{CM} = \frac{e^2}{C_M}\left(\frac{C_1 C_2}{C_M^2} - 1\right)^{-1}. \tag{4.8}$$

The honeycomb charge stability diagram includes the splitting of the original vertices (where energy levels were aligned) into a pair of "triple-points," so named as they correspond to gate values where there exists an energy degeneracy between three distinct charge configurations (as labeled in Fig. 4.5d). Again, these are points where energy levels are resonantly aligned between the dots, and are the only points for a series double quantum dot where transport is allowed through real states.

It is useful to define the chemical potential for each dot and a given electron configuration (N_1, N_2) as

$$\mu_1 = U(N_1, N_2) - U(N_1 - 1, N_2) \tag{4.9}$$

$$\mu_1 = \frac{1}{2}(N_1 - \frac{1}{2})E_{C1} + N_2 E_{CM} - \frac{1}{e}\left(C_{G1}V_{G1}E_{C1} + C_{G2}V_{G2}E_{C2}\right) \tag{4.10}$$

where C_{Gi} is the capacitance of gate i to dot i, etc. One notes

$$\mu_1(N_1 + 1, N_2) - \mu_1(N_1, N_2) = E_{C1} \tag{4.11}$$

$$\mu_1(N_1, N_2 + 1) - \mu_1(N_1, N_2) = E_{CM} \tag{4.12}$$

and may now relate the dimensions of the honeycomb cell in applied gate voltage to device capacitances. Along the honeycomb edges the chemical potential of the appropriate dot is aligned with the Fermi level of the leads, and hence $\mu = 0$. Therefore we may equate $\mu_1(N_1, N_2; V_{G1}, V_{G2}) = \mu_1(N_1 + 1, N_2; V_{G1} + \Delta V_{G1}, V_{G2})$ and $\mu_1(N_1, N_2; V_{G1}, V_{G2}) = \mu_1(N_1, N_2 + 1; V_{G1} + \Delta V_{G1}^M, V_{G2})$ to find

$$\Delta V_{G1} = \frac{|e|}{C_{G1}}, \quad \Delta V_{G1}^M = \frac{|e| C_M}{C_{G1} C_2} \tag{4.13}$$

where $C_{1(2)}$ is the total capacitance of dot 1(2), and similarly for dot 2. The presence of a finite level spacing renormalizes the honeycomb cell size as $\Delta V_{G1(2)} = \frac{|e|}{C_{G1(2)}}\left(1 + \Delta/E_{C1(2)}\right)$.

4.3.2 Measurements at finite V_{SD}

Applying a finite dc V_{SD} causes the triple points to expand into triangular regions as the dot chemical potentials may fall anywhere within the bias window and still allow transport. This is illustrated in Fig. 4.5e. At the extrema of each quadrant in the figure we sit in a honeycomb cell with fixed charge number. Representative dot chemical potential values are illustrated in the figure, with dotted lines representing the zero-bias honeycomb boundaries.

Resonant energy level alignment between the two dots occurs only along a line parallel to that connecting the original triple points. In addition, excited state resonant alignment may occur in the body of the triangles, appearing schematically as lines in the lower triangle of Fig. 4.5e. These resonances may be due to the alignment of two excited states, or of one excited state with the ground state of the other dot. Schematic level diagrams appear in the figure to illustrate these effects. It is also common to find off-resonance conduction in the body of the finite bias triangles due to either cotunneling or phonon emission [57] (for further discussion, see chapter 5).

Using an analysis similar to that in section 4.3.1 we utilize the size of the finite bias triangles to extract the final capacitance ratios necessary to calculate all germane capacitances for both dots. Such a calculation gives $\delta V_{G1(2)} = \frac{C_{1(2)}}{C_{G1(2)}} V_{SD}$.

4.3.3 The effect of interdot tunnel coupling

Similar to a mutual capacitance, the addition of finite tunnel coupling $|t|$ between a pair of quantum dots leads to a splitting of the original vertices in the square charge stability diagram. Each line represents the single particle ground state energy for a particular dot (dotted lines, Fig. 4.5f), $E_{1(2)}$. In the basis of dot 1/dot 2 occupation, the addition of tunnel coupling adds off-diagonal matrix elements to the system Hamiltonian as

$$H = \begin{pmatrix} E_1 & t_{21} \\ t_{12} & E_2 \end{pmatrix}. \tag{4.14}$$

Diagonalization of this Hamiltonian results in “bonding” and “antibonding” energies $E = \frac{1}{2}(E_1 + E_2) \pm \sqrt{\frac{1}{4}(\Delta E)^2 + |t_{12}|^2}$. These two energies are shown schematically in Fig. 4.5f, as hyperbolas which approach the original states $E_{1(2)}$ asymptotically in ΔE. At zero detuning the energy splitting is given by $2|t_{12}|$, and expands with increased ΔE. In the presence of a mutual capacitance, the two forms of triple-point splitting act additively, and the relative components of the splitting must be determined independently.

Chapter 5

Local gate control of a carbon nanotube double quantum dot

5.1 Introduction

Carbon nanotubes have been considered leading candidates for nanoscale electronic applications [44, 127]. Previous measurements of nanotube electronics have shown electron confinement (quantum dot) effects such as single-electron charging and energy-level quantization [146, 25, 91]. Nanotube properties such as long spin lifetimes make them ideal candidates for spin-based quantum computation based on double quantum dots [105] or multiple series quantum dots [47]. However, realizing such devices requires independent gate control over multiple charges and spins. This ability has not been achieved in previous measurements, where device properties were controlled with a single global gate such as the doped silicon substrate [80, 98]. We report the fabrication and measurement of a nanotube-based double quantum dot

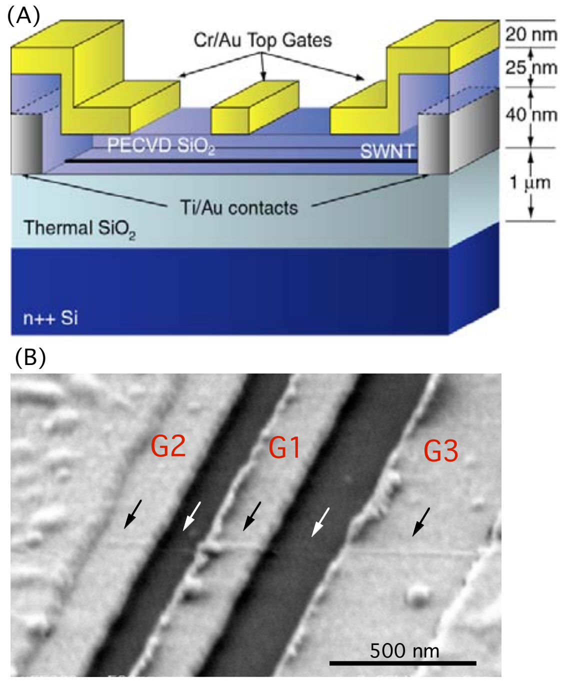

Figure 5.1: A) Schematic of top-gated device. B) Electron micrograph of a representative device. Arrows indicate the embedded nanotube.

with multiple, independent gates. The gates are used to manipulate and study single electron charging as well as charge interactions, and relevant device parameters are extracted directly from transport data.

The device under study consists of a nanotube $\sim$ 2 nm in diameter of length L $\sim$ 1.5 mm between metal contacts, with three top gates [21, 167] and a doped Si backgate (Fig. 5.1). Room temperature measurements of conductance as a function of any gate voltage indicate that the nanotube is either metallic with a strong resonance or a small band-gap semiconductor. At low temperatures, single electron charging is observed as Coulomb blockade conductance peaks, measured as a function of applied gate voltages. The observed peak pattern is different for each gate, and in some regions shows considerable super-structure, which appears with increasing source-drain voltage, V_{SD}. We observe a double periodicity of Coulomb charging phenomena, which is consistent with a nanotube quantum dot, defined by tunnel barriers to the leads, that has been split into two dots of roughly equal size by a defect in the middle of the device. (Measurements of conductance as function of bias voltage and gate voltage show Coulomb blockade with two nearly equivalent charging energies, indicating the two dots are of equal size. The symmetry of the honeycombs in Fig. 5.2 also indicates that the charging energies of the two dots are nearly equal). Structural defects often create tunable tunnel barriers [26, 34, 92, 36], and typically appear in nanotubes longer than ~ 200 nm. While such defects can be controllably fabricated [20], in this case the defect is inherent to the tube. The resulting dots each have a quantized energy level spacing of $\Delta = hv_F/2L \sim 1$ meV (assuming only spin degeneracy) where $v_F = 8.1 \times 10^5$ m/s is the Fermi velocity for a metallic nanotube [25].

5.2 Materials and methods

Carbon nanotubes were grown via chemical vapor deposition (CVD) from Fe catalyst islands using methane as a carbon source on a Si wafer. Nanotubes are located using an atomic force microscope and selectively contacted with Ti/Au leads (25nm/15nm), using electron beam lithography and liftoff. The devices are then coated with insulating SiO2 deposited via plasma enhanced chemical vapor deposition (PECVD) at room temperature. This technique is found to produce a high quality oxide films that does not damage the nanotube devices. Cr/Au top gates (200 nm x 20 nm) are subsequently aligned and patterned over the oxide-covered nanotube device, again, using electron-beam lithography and liftoff. In the device discussed, gates G1 and G3 cover the nanotube-metal contacts and G2 covers a middle section of the tube. The n++ Si substrate forms the backgate (Fig. 5.1). Numerous samples have been produced in this geometry, with a typical yield of 75% functional devices (with $\sim$ 10 total per chip) at the end of the fabrication process. One device is reported in detail here, although similar results have been obtained on others. The structural defect producing the double dot in this system does not generally appear in devices fabricated as above.

Measurements were made a ^{3}He cryostat, at a temperature of $\sim$ 320 mK, where Coulomb blockade is evident as a function of top gate voltages V_{G1} and V_{G2}, as well as backgate voltage V_{BG} (gate G3 was not used). Conductance was measured by sourcing a dc voltage and measuring dc current with an Ithaco 1211 current preamp and a digital multimeter. Differential conductance is measured using standard ac lock in techniques.

5.3 Transport characteristics

5.3.1 Honeycomb charge stability diagrams

The top gate voltages have differential capacitive coupling to the quantized energy levels of the two dots. Transport measurements indicate that gate G1 predominantly couples to dot 1 and gate G2 to dot 2. In the transconductance, dI/dV_{G1}, as a function of V_{G1} and V_{G2} (Fig. 2A), paired regions of large dI/dV_{G1} appear on the vertices of a hexagonal lattice. The resulting honeycomb-shaped array of high dI/dV_{G1} can be contrasted with the straight lines that would appear if each applied gate voltage coupled equally to the dots. The observed pattern strongly resembles the charge stability diagram for a found for weakly tunneling double quantum dot (inter-dot tunneling $\ll 2e^2/h$), where each cell of the honeycomb corresponds to a well-defined electron configuration for the double dot [154]. The vertex pairs are points of degeneracy between the two dots that have split because of inter-dot coupling (either capacitive or tunneling). At these vertices, energy levels resonantly align between the dots as well as the leads (Fig. 5.2C). For a series double dot, resonant transport only occurs at the vertices; finite non-resonant conductance along the edges of the honeycomb cells (Figs. 5.2D-E) occurs via cotunneling, which is suppressed in the weak-tunneling regime [154].

5.3.2 Vertices at finite dc bias

At finite bias, the vertex points expand into triangular regions (Fig. 5.2B) defined by lines where the energy levels of each dot align with either the top or bottom of the bias window. According to theory, resonant tunneling should occur only along the one side of the triangle that connects the original vertices. The observation of off-resonance tunneling in the body of the triangles has previously been attributed to both inelastic phonon contributions and cotunneling processes [153, 57, 9]. Because it appears that cotunneling is suppressed in this region (we do not see conduction along the edges of the honeycomb), conductance inside the finite-bias triangles suggests, perhaps, a significant contribution from electron-phonon coupling to transport. However, this conclusion appears inconsistent with the predicted suppression of electron-

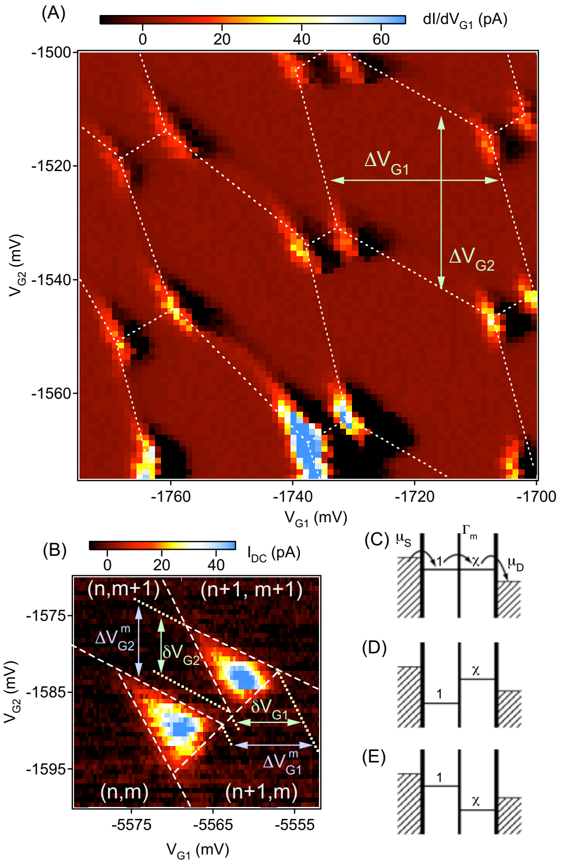

Figure 5.2: Experimental charge stability diagrams for the series double quantum dot as a function of two gate voltages, each shifting the energy levels of a single dot. Voltages V_{G1} and V_{G2} are divided by five before being applied to the gates of the device. (A) Color scale displays dI/dV_{G1} calculated from dc current (I_{DC}) at $V_{SD} =$ 500 μV. White lines are guides to the eye showing the honeycomb pattern of peaks in conductance. Vertex pairs correspond to points of degeneracy between the two dots where resonant transport occurs, while cotunneling may produce finite conductance along the honeycomb edges. B) Zoom-in of a vertex pair at $V_{SD} = 500$ μV with lines of constant energy designated by white dashed lines. Colorscale displays I_{DC}. Vertex dimensions are indicated on the diagram, as are particular electron configurations on the two dots for different regions of gate space. Note the triangular shape resulting from finite V_{SD}, and nonzero off-resonance conductance within the triangles. C) Level diagrams for a double quantum dot depicting resonant transport with Γ_m the inter-dot tunnel rate. The bias window $V_{SD} = (\mu_S - \mu_S)/e$, D-E) Level diagrams depicting configurations where cotunneling may contribute to transport.

phonon coupling in nanotubes at low temperatures [76, 158]. It seems more likely that inelastic processes are occurring via electron interactions with the source/drain reservoirs or the substrate. Figure 5.2B does not show resonant excited-state levels inside the finite-bias triangles, as are observed in lateral quantum dots [154]. This is not surprising, as $eV_{SD} < \Delta$ in the present case. Increasing V_{SD} causes the triangles to grow, as expected, but also inhibits our ability to resolve individual vertices and even individual honeycomb cells. Overall, however, the transport characteristics of this nanotube double dot are qualitatively similar to those observed for double dots fabricated in semiconductor heterostructures [153, 104]. Such similarities suggest that more complex quantum devices formed from molecular conductors such as nanotubes will continue to share features with well-studied semiconductor quantum dot systems. However, the larger energy scales in carbon nanotubes allows operation at higher temperatures.

5.4 Extraction of device parameters from transport

5.4.1 Dot capacitances

Double dot capacitances are obtained by measuring the sizes and separations of the honeycombs and vertices (Fig. 5.2) [154]. The size of the honeycomb in Fig. 5.2A determines $\Delta V_{G1(2)}$, where $\Delta V_{G1(2)} = \frac{|e|}{C_{G1(2)}}(1+\Delta/E_{C1(2)})$ with $C_{G1(2)}$ the capacitance of dot 1(2) to gate 1(2) and $E_{C1(2)}) \sim 2$ meV the charging energy for dot 1(2). $E_{C1(2)}) \sim$ is determined from $|eV_{SD}|$ measured at the apex of a conductance diamond in a plot of conductance as a function of V_{SD} and any gate voltage (not shown). From the size of the finite-bias triangles in Fig. 5.2B we determine capacitance ratios using $\delta V_{G1(2)} = \frac{C_{1(2)}}{C_{G1(2)}} V_{SD}$. With the above relationships we calculate typical dot capacitances of $C_{1(2)} \sim 160$ aF and $C_{G1(2)} \sim 45$ aF.

5.4.2 Interdot interaction

The amount of capacitive coupling and inter-dot tunneling can be determined from the vertex splitting [94, 86]. These couplings cause an energy shift related to the formation of charge polarized, or "bonding," states between the quantum dots (tunnel coupling is analogous to covalent bonding and capacitive coupling to ionic bonding). Both coupling parameters can be tuned with gate voltages that open the inter-dot constriction, so it is difficult to determine their relative contributions to vertex splitting. If we assume the vertex splitting is due to capacitive coupling alone, we find a mutual capacitance between dots $C_m \sim 90$ aF, using $\Delta V^m_{G1(2)} = \frac{|e| C_m}{C_{G1(2)} C_{2(1)}}$, where $\Delta V^m_{G1(2)}$ is the horizontal (vertical) component of the diagonal splitting measured between vertices [154]. A separate determination of the mutual capacitance based on single-dot capacitances (determined above) and the magnitude of the charging energy using the relation $E_{C1(2)} = \frac{e^2}{C_{1(2)}}(1 - C_m^2/C_1 C_2)^{-1}$ gives $C_m \sim 100$ aF. The similarity between these two values for Cm indicates that the vertex splitting in this region is dominated by capacitive coupling. The interaction energy is then approximately $E_m = \frac{e^2}{C_m}(C_1 C_2/C_m^2 - 1)^{-1} \sim 700$ μeV.

Opening the inter-dot constriction is expected to increase the tunnel coupling exponentially faster than the capacitive coupling [94]. We can therefore compare

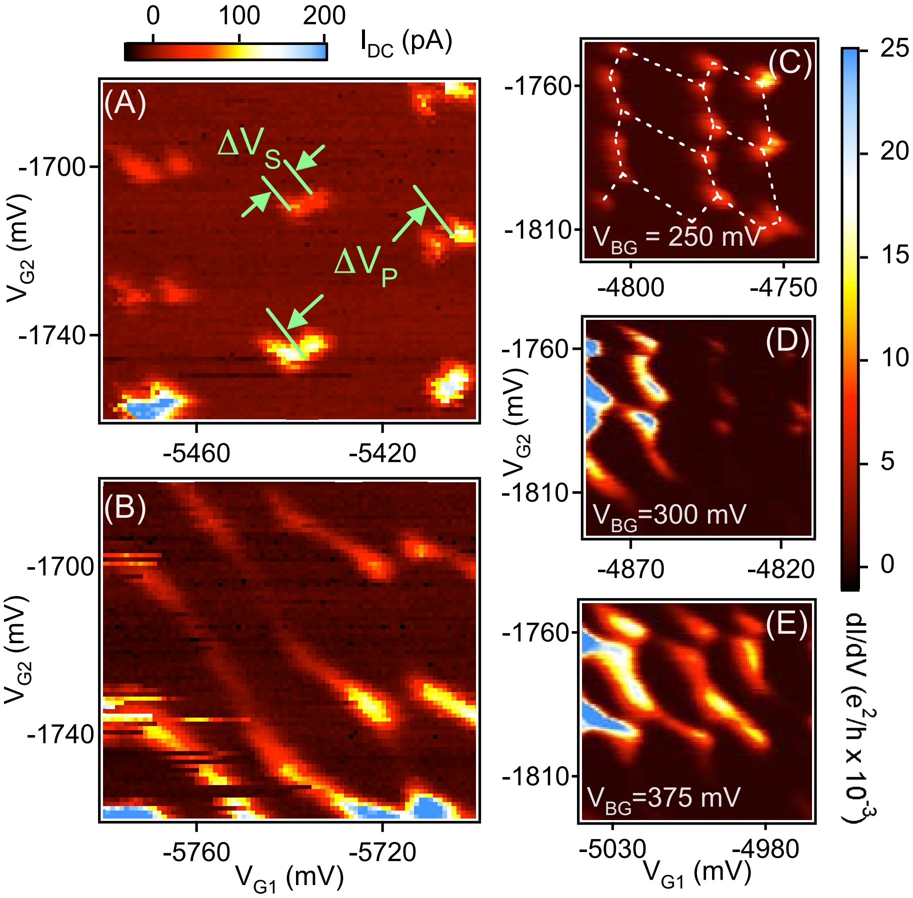

Figure 5.3: A) Experimental charge stability diagram demonstrating weak interdot tunnel coupling. $V_{SD} = 500\ \mu$V. Vertex peak splitting (ΔV_S) and honeycomb cell dimensions (ΔV_P) indicated on the plot. B) Moving to a different region of V_{G1} changes the tunnel coupling between dots, producing a smeared charge stability diagram. C-E) Experimental stability diagrams for fixed charge configuration at various V_{BG}. $V_{SD} = 800\ \mu$V. The capacitive coupling of the backgate to the two dots requires that slightly different ranges of V_{G1} and V_{G2} be used to cover the same charge configurations at different V_{BG} values.

the amount of inter-dot tunnel coupling in different gate configurations using the fractional peak splitting, defined $f = 2\Delta V_S/\Delta V_P$ where ΔV_S is the diagonal splitting measured between vertices and ΔV_P is the distance between vertex pairs (Fig. 5.3A) [104]. A value of $f = 1$ corresponds to a transparent inter-dot constriction, while $f = 0$ indicates two isolated dots in the limit of zero mutual capacitance between dots. Changes in f, however, should be dominated by tunnel-coupling, so measuring how f changes as a function of gate voltage allows the contribution to the vertex splitting from inter-dot tunneling to be inferred. We observe an evolution of f by holding the range of V_{G2} fixed and examining different regimes of V_{G1} (Figs. 5.3A-B). In Fig. 5.3A, where honeycomb cells and vertices are well defined, we find that $f \sim 0.3$. This regime can be contrasted with that of Fig. 5.3B, where an increase in inter-dot tunnel coupling leads to a smearing of vertices and honeycomb cells. In this region, vertex splitting grows to a value of $f \sim 0.7$.

In Figs. 5.3C-E we use a combination of V_{G1} and V_{G2} to maintain a fixed electron configuration while tuning tunneling with the backgate. The evolution evident here shows how varying V_{BG} from 250 mV to 375 mV changes our stability diagram from weak to strong cotunneling regimes. The corresponding increase in vertex heights indicates that we are also influencing the total amount of tunneling through the double-dot. Because the vertex splitting does not change significantly, it seems that the backgate is primarily tuning the transparency of the tunnel barriers at the source and/or drain electrodes [26].

5.5 Temperature dependence of CB peaks

Increasing temperature increases cotunneling conductance (i.e. conductance on honeycomb edges) by a relation well described by a power-law, $G_{cot} \propto T^{\eta}$, over the range investigated,where η is between 1 and 2 with a typical value of $\eta \sim 1.3$

(Fig. 5.4A and Fig. 5.4C, upper curve). In contrast, resonant vertex peak conductance is roughly independent of temperature, or only slightly increases with increasing temperature (Fig. 5.4B and Fig. 5.4C, lower curve). Power law behavior with $\eta = 2$ has been predicted for cotunneling peaks in the weak inter-dot tunneling regime ($G_{int} \ll e^2/h$) at low temperatures ($k_B T \ll \Delta$) [114]. A power law with $\eta = 1.25$ — comparable to what we find — is predicted [114] for intermediate tunnel coupling and $\Delta \ll k_B T$ (corresponding to temperatures higher than those of our measurements). The nearly temperature-independent behavior we observe for resonant peaks does not appear consistent with predictions of peak height scaling as as $1/T$ in the low-temperature regime [86] ($1/T$ behavior is expected for $G < k_B T \ll \Delta$). Given that other measurements of this system correspond relatively well to predicted behavior, it is surprising that the temperature dependence deviates so far from theoretical expectations. These unexplained features will be investigated in future experiments employing controlled defect placement along with local gating.

5.6 Acknowledgements

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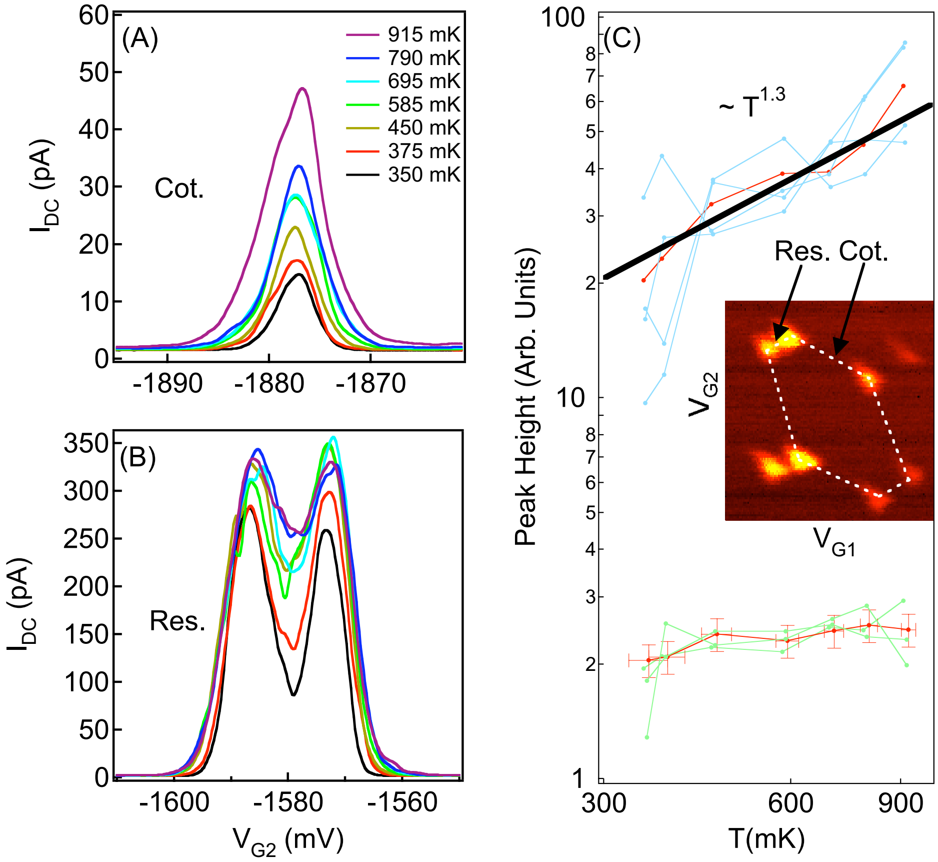

Figure 5.4: Temperature dependence of peak heights for two different regimes of transport. One-dimensional sweeps taken in V_{G2} with V_{G1}= -1800 mV. Representative cotunneling peak (A), denoted “Cot.” and vertex peaks (B), denoted “Res.”, at temperatures between T = 350 mK and 915 mK. C) Peak height as a function of temperature on a log-log plot. Peaks are sorted by type (resonant or cotunneling) into two distinct groups, and have all been offset to collapse approximately onto a single curve for each group. The black line shows the average power law behavior, $T^{1.3}$, for cotunneling peaks. Peaks shown in (A) and (B) are shown in red. Inset) Representative honeycomb cell in the region of measurement.

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Chapter 6

Locally addressable tunnel barriers within a carbon nanotube

6.1 Introduction

Carbon nanotubes are a leading material system for molecular electronic device applications as well as for fundamental studies of the electronic properties of low-dimensional systems. Single-walled carbon nanotubes can function as nanoscale analogues of electronic elements such as field-effect transistors [147, 110, 11, 167, 166] and interconnects [75, 100] in integrated circuits. In addition, nanotubes behave as ballistic conductors with large current density capacity, and also display single electron (quantum dot) charging and quantum effects at low temperatures [26, 35, 79, 117, 124, 143]. Conformational changes in nanotubes modify their electronic properties: devices such as diodes have been created using intra-tube tunnel barriers formed from mechanically induced defects or“kinks” [130, 131, 27]. Scanned-gate microscopy indicates that the kinks serve as scattering centers[26, 27] consistent with theoretical predictions for bending defects in nanotubes[33, 118]. The properties of individual tunnel barriers were not independently adjustable in previous studies, however, as only a single backgate was available.

In this section we describe the realization of locally-addressable, fully-tunable tunnel barriers within a single carbon nanotube. We study tunnel barrier formation in nanotubes contacted with Ti/Au and Pd for comparison. In the former case, the barriers are due to bending defects, formed by mechanically kinking the nanotube with an atomic force microscope [130]. We show that electrostatic gates placed near each of the kinks independently tune these tunnel barriers from transparent to opaque, whereas gates placed away from the kinks (over undeformed sections of the nanotube) have little or no effect. Previous studies have shown that spatially localized electrostatic gates can deplete the middle of a nanotube device [166], or tune naturally occurring scattering centers within a nanotube [21]. The results presented in subsection 6.2.2 and highlight the role of mechanical defects in creating such localized scattering centers and in determining the transport characteristics of carbon nanotube devices. In addition, the ability to manipulate defects provides another level of device control, along with the application of spatially localized electrostatic gates.

In contrast, devices contacted with Pd electrodes may be depleted locally, without the fabrication of mechanical defects along the length of the nanotube. We describe this effect and postulate a mechanism for the difference between these two sets of experiments.

6.2 Mechanically deformed tubes contacted with Ti/Au

6.2.1 Methods

Carbon nanotubes were grown via chemical vapor deposition from patterned Fe catalyst islands on a degenerately doped Si/SiO$_2$ wafer, using methane as the carbon source19. After locating a target nanotube with an atomic force microscope (in conventional raster mode), the cantilever tip was lowered and then used to push the nanotube laterally under computer control. The resulting kinks had slightly different shapes, with typical lateral deviations of $\sim$ 200 nm from their undisturbed (i.e., straight) configuration. After kinking, the nanotubes were contacted with Ti/Au electrodes, forming devices of length $\sim$ 1–2 μm. The wafers were then coated (without patterning) with $\sim$ 25 nm SiO2 deposited via plasma-enhanced chemical vapor deposition [111]. Multiple Cr/Au top gates ($\sim$ 200–300 nm across, $\sim$ 40 nm thick), patterned using electron beam lithography and lift-off, were positioned over each tube, with a gate placed near each kink and at least one additional gate over an unkinked section of the same nanotube as a control. In addition, the doped Si substrate was used as a global backgate.

6.2.2 Single kink device

We first discuss a device with one kink and three top gates, one gate near a kink (G2) and two gates over unkinked sections of the nanotube (G1 and G3), as shown in the inset to Fig. 6.1a. Two-terminal conductance is measured from 1.7 K to 300 K using a voltage bias of 10 mV and measuring dc current using an Ithaco 1211 current amplifier and digital voltmeter. All gates are connected to dc voltage sources, and are set to 0 V (relative to tube ground) unless otherwise specified. Measurements of conductance as a function of backgate voltage, V_{BG}, at room temperature show field-effect behavior consistent with p-type doping. Setting $V_{BG} = 0$ V and applying a voltage, V_{G2}, to G2 gives a strong gate response, while applying voltages V_{G1} and V_{G3} to gates G1 and G3 produces little change in conductance (Fig. 6.1a). In the latter case, the voltage applied to G2 determines the value of this nearly constant conductance. These results, as well as those below, demonstrate the local effect of the top gates. The lack of gate response to G1 and G3 demonstrates that the field-effect behavior observed as a function of V_{BG} is likely not due to a depletion of the bulk of the nanotube. In addition, we find that at temperatures below ~ 200 K the backgate has little effect on conductance.

At temperatures below ~ 135 K, regions of charges confined by one or more kinks give rise to Coulomb blockade oscillations in conductance as a function of various gate voltages. In this Coulomb blockade regime, measurements of conductance as a function of V_{G2} and dc bias, VSD, produce a series of irregular diamonds (Fig. 6.1b), suggesting that the single kink defines several small quantum dots (i.e., the device has two or more barriers). Previous experiments have established that closely spaced mechanical defects can create quantum dots [131, 27]. Measurements of the conductance diamonds show that the dots in our device have a large charging energy (>20 meV) (The typical charging energy is determined by finding the apex of a single electron diamond in a 2D plot of current or conductance as a function of bias

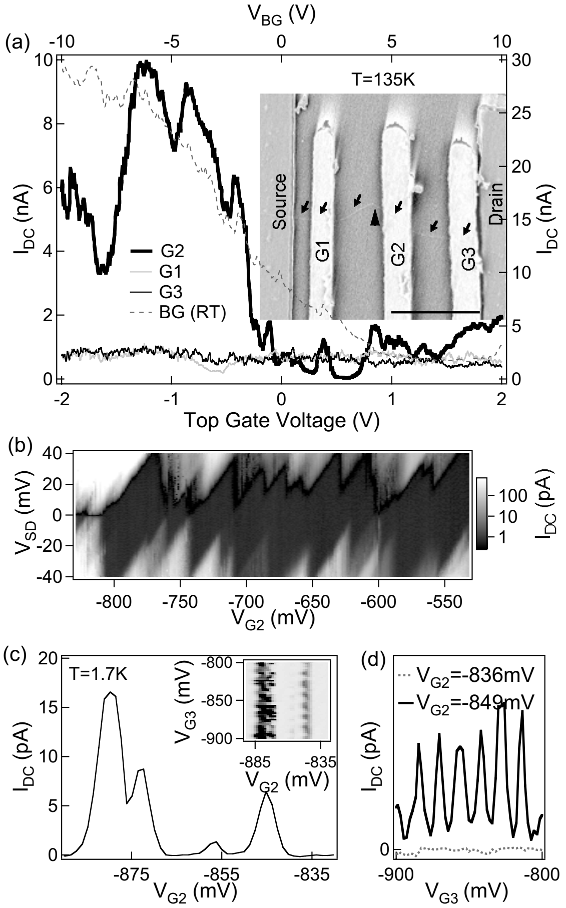

Figure 6.1: (a) Gate response of single-kink device measured at T=135 K. Plot shows dc current as a function of three gate voltages, V_{G1}, V_{G2} and V_{G3} over different sections of the nanotube, (bottom, left axes) and of V_{BG} at room temperature (top, right axes). Inset: SEM image of the device with small arrows indicating the position of the nanotube under the SiO_2 insulating layer and large arrowhead indicating the location of the kink. Scale bar $\sim$ 500nm. (b) Absolute value of dc current as a function of V_{SD} and V_{G2} presented on a logarithmic grayscale showing irregular Coulomb diamonds with charging energies > 20 meV. (c) Gate response of kinked device to V_{G2} (over kink) at low temperature showing Coulomb charging. Inset: Grayscale plot of dc current as a function of V_{G2} and V_{G3} displaying resonant transport through multiple dots in series. Fig. 1(d) Horizontal slices through grayscale plot in Fig. 1(b) at on- and off-peak values for V_{G2}. On peak shows coulomb blockade as a function of V_{G3} while off-peak shows total suppression of current.

voltage and gate voltage (as in Fig. 6.1b)). Because the diamonds do not close near zero bias, we measure current or conductance at larger dc biases. Figure 1c shows irregularly spaced Coulomb blockade peaks that appear when V_{G2} is swept at 1.7 K and V_{SD}=10 mV. We note that the applied dc bias is smaller than the typical charging energy measured as above. With V_{G2} tuned to a conductance peak, Coulomb oscillations are seen as a function of either V_{G3} or V_{G1} on a gate-voltage scale different from that measured for V_{G2} (Inset Fig. 6.1c, Fig. 6.1d). This is consistent with additional quantum dots forming between the defect and tunnel barriers at the contacts [146, 35], with energy levels modulated by V_{G1} and V_{G3}. In this case, resonant transport occurs only when the energy levels between all dots (source-kink, kink, kink-drain) are resonantly aligned. At V_{G1}=0V the source-kink dot is transparent; the resulting double-dot system is evident in a two-dimensional plot of dc current as a function of V_{G2} and V_{G3} (inset to Figure 6.1c). The pattern of alternating high and low conductance regions is due to energy levels moving in and out of resonant alignment between the two dots [154].

6.2.3 Double kink device

We next discuss a device with multiple kinks, each with a nearby gate. The inset to Figure 6.2 shows a realistic schematic of a device with two gated kinks (under G4 and G6) and an additional top gate (G5) over the section of the nanotube between the kinks. Room temperature measurements show a strong response to V_{BG} (Fig. 6.2a). When V_{BG} is swept below ∼ 150 K (here at 70 K) the field-effect behavior is superposed with irregular oscillations. In this device we find an appreciable effect

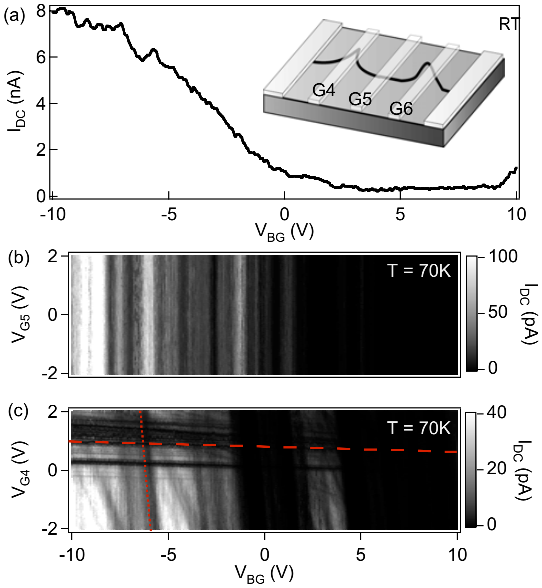

Figure 6.2: (a) Room temperature conductance of double-kink device displaying approximate p-type field-effect behavior. Inset: Schematic of double kink device, showing kinks of different shapes and bending angles. (b) Grayscale plot of dc current as a function of V_{BG} and V_{G5} at T = 70 K. Coulomb oscillations appear in V_{BG}, but no effect of V_{G5} is evident. (c) dc current as a function of V_{BG} and V_{G4} showing the ability to tune transport through gate control of a kink. Two scales of voltage additivity are present, indicated by dotted and dashed lines.

of sweeping V_{BG} at low temperatures, in contrast to the device discussed earlier. The top gates in this device are $\sim$ 100 nm wide, compared to $\sim$ 200 nm gates for the device in Figure 6.1, and therefore may produce less screening of the backgate over the deformed sections of the tube. At temperatures below $\sim$ 30 K we are unable to measure conductance within applied dc biases and gate voltages, likely because the formation of multiple quantum dots along the length of the nanotube inhibits transport. A two-dimensional plot of dc current (V_{SD}=10 mV) as a function of V_{BG} and V_{G5} shows the negligible effect of V_{G5} (Fig. 2b). In contrast, measurements of dc current as a function of V_{BG} and V_{G4} show a strong gate response to V_{G4}. The nearly horizontal features visible in Fig. 6.2c correspond to values of V_{G4} at which transport is suppressed by reducing the transparency of the underlying kink. The dashed line points out one such feature, which has a slight slope because of capacitive coupling between the backgate and the kink. Oscillatory features as a function of V_{BG} persist, again with a slope (dotted line) due to coupling between V_{G4} and V_{BG}. The slope indicates that the V_{G4} and V_{BG} may be affecting the same sections of the nanotube, and that the effect of V_{G4} may not be restricted to the proximal section of the nanotube directly under the gate.

Local control over individual kinks is demonstrated in Figure 6.3a, where dc current (V_{SD}=10 mV) is plotted as a function of V_{G4} and V_{G6}. To maximize conductance we set V_{BG}=-10 V. When both V_{G4} and V_{G6} are large and negative, current through the device is large, indicating that both kinks are transparent. Beyond this corner of the plot, conductance is strongly suppressed by either of the two top-gate voltages. The sharp turn-on of the double-kink device in response to multiple input voltages

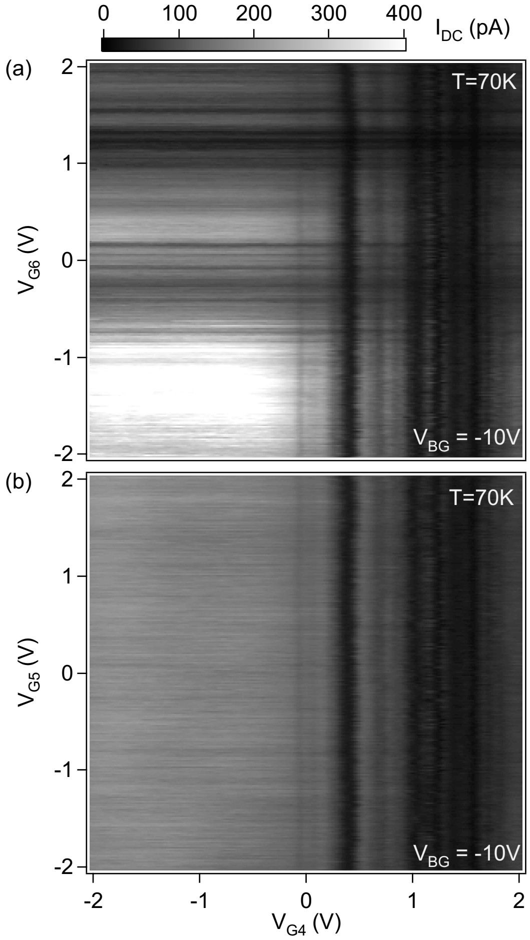

Figure 6.3: (a) dc current as a function of V_{G4} and V_{G6}, both over kinks in the nanotube, demonstrating the ability to inhibit transport through the device by appropriately tuning either kink. (b) dc current as a function of V_{G5} and V_{G4}. V_{G5} has almost no effect on transport through the device.

is equivalent to an AND logic element. The appearance of perpendicular horizontal and vertical bands indicates that G4 and G6 have very little cross-capacitance. Measurements at smaller negative backgate voltages produce similar features with a suppressed current flow. Measurements of dc current as a function of V_{G4} and V_{G5} produce the same features in response to V_{G4}, but show no response to V_{G5} (Fig. 6.3b). Despite differences in the shapes of the three kinks studied here, we note that all respond to gate voltages on approximately the same scale.

6.3 Semiconducting tubes contacted with Pd

Nanotubes contacted ohmically using Pd demonstrated considerably different behavior than those contacted with Ti/Au. Top-gated devices fabricated as described in Section 3.2.3 using Pd as a contact material showed carrier depletion, and hence a suppression of conductance as a function of any applied top-gate voltage, without the need for mechanical deformation of the tube.

The difference between Ti/Au and Pd contacted nanotubes may be due to decreased band bending in Pd contacted tubes, as the valence band edge in a semiconducting nanotube is very close to the work function of Pd, while the offset between the tube band edge and metal work function is much larger in the case of Ti contacts [22]. In fact, considerable experimental effort has been invested in the operation of Ti/Au contacted nanotubes as Schottky barrier transistors [74], consistent with our experimental findings.

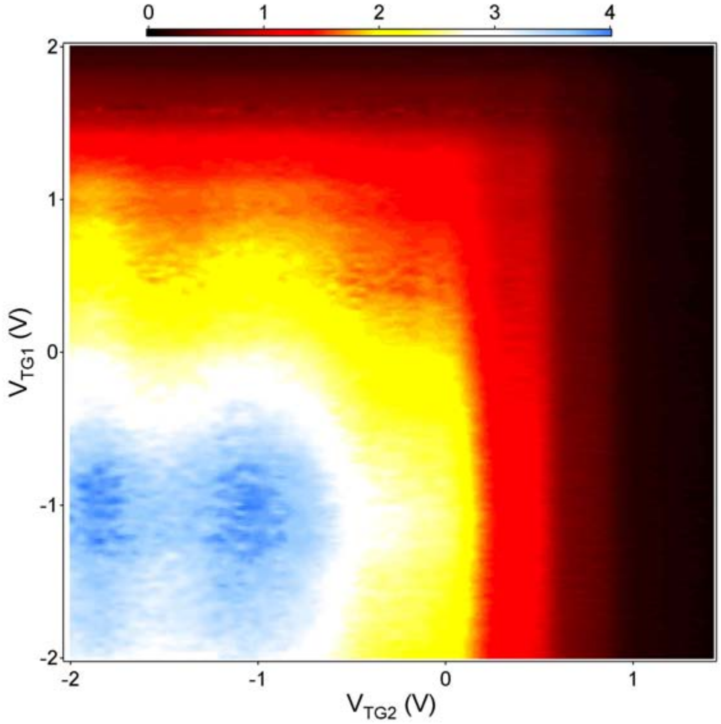

Figure 6.4: Differential conductance (color scale, units e^2/h after subtraction of series resistance $R_S = 34k\Omega$) as a function of two independent top-gate voltages with dc $V_{SD} = 36$ mV. The appearance of a corner instead of diagonal structure indicates that the two gates act independently and can each suppress conductance with appropriate biasing.

6.4 Conclusions and acknowledgements

In conclusion, we have fabricated and investigated nanotube devices with intentional bends and kinks created using an atomic force microscope, and electrostatic top gates near the kinks. These kinks behave as controllable tunnel barriers with local gate addressability. In contrast, gates placed away from the kinks on the same nanotubes had little or no effect on conductance. It is possible, however, that gates placed away from the kinks could affect conduction, or locally deplete the nanotube, at higher voltage scales than the ones we studied, or with different contact materials. In fact, we find that when nanotubes are contacted with Pd we are able to locally deplete any section of the tube. The results of these experiments highlight the role of defects and local scattering centers in the transport properties of nanotubes, and suggest that other recent results on top-gated nanotube FETs contacted with Ti/Au leads may rely on inherent local scattering centers to deplete the middle of the nanotubes [166]. Further, the fact that carrier depletion in Pd contacted nanotubes occurs at different voltages for different top-gates suggests a nonuniform band model of a nanotube where defects locally deform the potential along the nanotube length.

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Chapter 7

Gate-defined intratube quantum dots

7.1 Introduction

A number of proposed solid-state devices [17, 93] take as their fundamental element the quantum dot-a classically isolated island of electrons with a discrete energy spectrum [17, 93]. As a substrate for realizing multiple quantum-dot devices, carbon nanotubes [78] offer a variety of appealing physical properties. However, nanotube-based electronics in general have been limited by the difficulty of fabricating complex devices on a single tube. In previous studies, isolated quantum dots formed in carbon nanotubes were defined either by tunnel barriers at the metal-nanotube interface [115, 125], or by intrinsic [26, 111] or induced [131, 20] defects along the tube. These devices demonstrated the potential of nanotube-based quantum devices but did not allow independent control over device parameters (e.g., charge number and tunnel barrier transparency), and also placed stringent geometric constraints on device design. In the present study, we address some of these challenges by forming the quantum dots on the nanotube using only patterned gates, while the contacts to the nanotube remain highly transparent. This design allows multiple quantum dots to be arbitrarily positioned along a tube (quantum dots connected to 1D nanotube leads), with independent control over tunnel barriers and dot charges. A backgate is used to set overall carrier density. Here, we show that quantum dots fabricated in this manner exhibit familiar characteristics, yet provide significant advances in device control. In particular, full control over tunnel barrier locations and transparencies should allow improvements in the study and control of spin and charge dynamics in carbon nanotubes.

7.2 Materials and Methods

Nanotubes were grown via chemical vapor deposition from lithographically defined Fe catalyst islands on a degenerately doped Si wafer with 1μm of thermally grown oxide (See Fig. 7.1a). Atomic force microscopy was used to locate nanotubes relative to alignment markers, and single-walled tubes with diameters less than ~ 3 nm were contacted with 15 nm of Pd, patterned by electron beam lithography [81]. Device lengths were in the range 5–25 μm. After contacting, the entire sample was coated with 25–35 nm of either SiO_2 deposited by plasma-enhanced chemical vapor deposition (PECVD) or Al_2O_3 deposited by atomic layer deposition (ALD). Cr/Au top-gates, 150–300 nm wide, were then patterned over the tubes using electron-beam lithography, with care taken to prevent overlap between the gates and the Pd contacts.

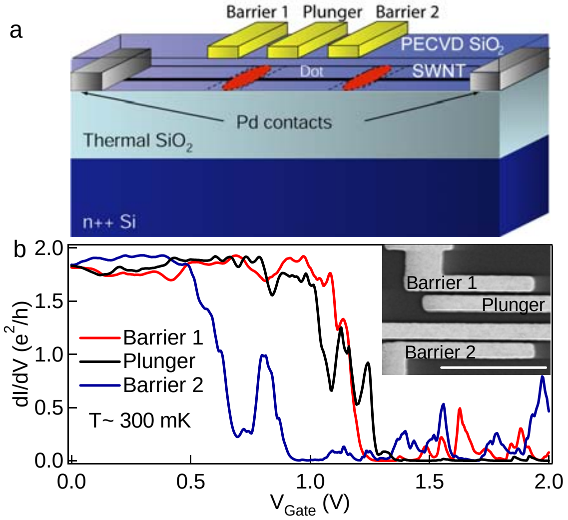

Figure 7.1: a) Schematic of a gate-defined carbon nanotube quantum dot showing vertically integrated geometry and ohmic contacts. Pd provides high-conductance contacts at the metal-nanotube interface which do not form tunnel barriers at low temperatures. b) Gate response of a $\sim$ 25 μm long nanotube contacted with Pd, top-gated using PECVD SiO_2 at $T \sim 300$ mK with $\sim$ 10 μV ac excitation. For this device, all gates strongly suppress conductance at voltages above $\sim +1$V. Inset: SEM of a lithographically similar gate pattern. The middle two gates are connected together and serve as a single plunger gate. Scale bar = 2 μm.

Two-terminal conductance was measured in either a pumped ^{4}He cryostat (300 K to 1.5 K) or a ^{3}He cryostat (300 K to 0.3 K). Current and differential conductance, dI/dV, were measured simultaneously using a combined ac + dc voltage bias with a current amplifier (Ithaco 1211) and lockin amplifier.

All semiconducting nanotubes coated with PECVD SiO_2 showed p-type field effect transistor behavior at room-temperature, exhibiting carrier depletion with positive voltage applied to top or back-gates (conductance was typically suppressed by three to four orders of magnitude at voltages of $\sim$ 1–3 V) [22]. In contrast, some tubes coated with ALD showed ambipolar behavior (high conductance at both positive and negative applied top or back-gate voltage surrounding a low-conductance region) with thermally activated conductance in the gap. We believe this difference may be due to oxygen doping of the nanotubes by the highly energetic oxygen plasma in the PECVD process. Room-temperature maximum conductances at zero dc bias, $V_{SD} = 0$, ranged from ~ 0.5–$2\ e^2/h$. Overall, devices coated with PECVD and ALD were qualitatively similar in behavior. Devices showing a relatively weak gate response (presumably metallic) were not investigated further.

7.3 Operation of gate-defined dots

7.3.1 Three-gate geometry for a single dot

Single quantum dots were formed using a three-gate configuration (Fig. 7.1a), where outer gates act as tunnel barriers defining the dot (denoted "barrier 1" and "barrier 2") by locally depleting carriers beneath them, and a center gate (denoted "plunger") shifts the chemical potential in the dot relative to the chemical potentials of the contacts and the segments of the tube away from the gates. Gate response of tube conductance (Fig. 7.1b) for a single-dot device using PECVD SiO_2 (micrograph of similar device shown in Fig. 7.1b, inset; the two center gates are connected and act as one plunger gate) shows p-type field effect behavior, that is, the tube is depleted when any top-gate bias becomes sufficiently positive. The gated region of the nanotube is $\sim 2\ \mu$m in length, while the total tube length is $\sim 25\ \mu$m between the Pd contacts.

Independent gate action

The independent action of the barrier gates is evident in the two-dimensional plot of differential conductance, dI/dV, as a function of barrier gate voltages, shown in Fig. 7.2a. The square edge of the conducting region demonstrates independent barrier depletion with little cross-coupling. Parallel diagonal features separated by $\sim$ 2 mV visible near the pinch-off of both barrier gates (Fig. 7.2b) are a signature of Coulomb blockade, discussed below. Figure 7.2b demonstrates that the barrier gate voltages can be controllably adjusted to allow a transition from open conduction to weak tunneling through a gate-defined quantum dot resulting in the appearance of Coulomb blockade peaks.

Coulomb blockade in a single dot

Examined as a function source-drain voltage bias, V_{SD}, as well as plunger gate voltage, the Coulomb blockade peaks form a series of repeated "Coulomb diamonds" where conduction is suppressed whenever the energy to add the next hole to the device exceeds V_{SD} (Fig. 7.2c). The ratio, $\eta^{-1} \sim 0.85$, of Coulomb diamond height (V_{SD}) to width (plunger voltage) gives the conversion, $e\eta$, from the distance in plunger voltage between Coulomb blockade peaks to the dot charging energy $E_C = e^2/C \sim e^2/\kappa\epsilon_0 L$ ($\kappa \sim 4$ is the dielectric constant of SiO_2), and indicates a strong coupling of the plunger gate to the dot [25]. From this analysis, one extracts a dot length of $L \sim 2$ mm, comparable to the length of the gated region of the tube, and much less than the $\sim$ 25 μm tube length. Several hundred consecutive Coulomb peaks are visible over a range of plunger gate voltage $>$ 4V. Throughout this range, peak heights remain

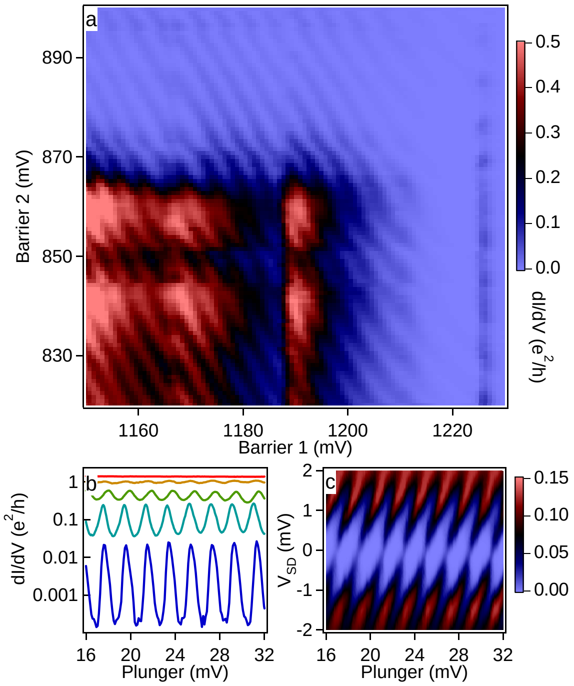

Figure 7.2: a) Differential conductance, dI/dV, plotted as a function of barrier gate voltages. Conductance can be suppressed by the application of either gate voltage, leading to the observed corner. Both barrier gates couple capacitively to the carrier densities in the proximal sections of the nanotube and also to the chemical potential of the dot formed between the depletion regions. Thus, near full pinch-off with both gates we observe the emergence of a series of diagonal lines in the 2D plot due to the onset of single electron charging. b) dI/dV on a logarithmic scale as a function of the plunger gate for various values of barrier gate voltages. Data measured on a subsequent cool down from those in panels a and c, where the exact position of the corner has shifted slightly in gate voltage. From bottom to top, data are taken at various barrier gate values falling along a diagonal line (with slope approximately 0.8 in the Barrier 1 - Barrier 2 plane) starting from the corner at which conductance is pinched off towards lower gate voltages where conductance is larger. At the highest barrier gate voltages, well-isolated Coulomb blockade peaks are observed; decreasing the barrier gate voltages yields Coulomb oscillations on a high conductance background and eventually open transport without charging effects. 2c. Differential conductance, dI/dV, (in units of e^2/h) as a function of plunger gate voltage and source-drain voltage, V_{SD}, for Barrier 1 (2) = 1200 (880) mV. Coulomb diamonds (regions of suppressed conductance) indicate where the charge on the dot is fixed.

controllable by adjusting the barrier gates.

7.3.2 Five-gate double dot

Taking advantage of the versatility of gate-defined devices, we next investigate a double quantum dot formed by three depletion regions along a nanotube. The double quantum dot, shown in Fig. 7.3a, comprises left and right barrier gates, a middle barrier gate and two independent plunger gates. Gates are approximately 150 nm wide with 150 nm spacing; total nanotube length is $\sim 10\ \mu$m, much longer than the double dot.

Transport in a double quantum dot

Resonant transport through double dots in series occurs only when available energy levels in each dot align with each other and with the chemical potentials in the two leads [154]. When the mutual capacitance of the dots is weak, the alignment condition occurs at the intersection of the Coulomb peaks leading to a rectangular grid of resonant conduction peaks. Such a pattern is seen in Fig. 7.3b. The resulting charge stability diagram forms approximately square cells, each corresponding to a fixed charge number in both dots. In the regime shown in Fig. 7.3b, cross-coupling of plunger gates, which would skew the square pattern into rhombus shapes, appears to be quite small. We note that these measurements were conducted at $T \sim 1.5$ K, higher than the typical temperature where double dots based on semiconductor heterostructures have been measured [154].

Control over interdot coupling

Gate voltages can also be used to control interdot coupling, allowing a transition from two isolated dots (uncoupled) to one large dot (fully coupled). Increasing the coupling between the two dots (by reducing the voltage on the middle gate) leads to a splitting of the high-conductance points of degeneracy between different charge configurations, and the emergence of a honeycomb pattern in the charge stability diagram (Fig. 7.3c). The interdot interaction may be due to capacitive or tunnel-coupling, but it has been shown that tunnel-coupling increases exponentially faster with a reduction of the interdot barrier [94]. In addition, as the voltage on the middle gate is reduced we observe an increase in vertex height by approximately an order of magnitude. It is therefore likely that finite tunnel coupling leads to the splitting of the vertices [163, 104] in Fig. 7.3c, which in this case is partially obscured by thermal broadening. (Any splitting of the charge degeneracy points in Fig. 7.3b is smaller than the thermal smearing.) In addition to the vertex splitting in Fig. 7.3c, we observe strong conductance along the edges of the honeycomb cells, due to higher-order processes through virtual states. Further decreasing the voltage on the middle gate yields a series of straight diagonal lines as a function of the two plunger gates, as expected when the two dots merge to form a single large dot. The lines arise from Coulomb charging where both gates act additively in coupling to the single particle states of the dot (Fig. 7.3d) [40]. An analysis of the spacing between the Coulomb peaks along the total energy axis (a line perpendicular to the sloped lines) shows that the peak spacing in Fig. 7.3d, 4.8 mV, is half of that required to move from one degeneracy point to the next along a similar line in Fig. 7.3b, 9.6 mV. This factor of two corresponds nearly exactly to the difference in the size of a single dot between the isolated and strongly coupled cases for this device, as peak spacing is inversely proportional to dot length [115]. The fact that a single dot can be formed by outside barriers, with three nominally inactive gates between them, suggests that there is little inadvertent depletion or tube damage from the deposition of these top gates.

Calculation of interdot tunnel coupling

Conductance through the double dot for different values of middle gate voltage is consistent with the interpretation that the interaction between the two dots is due to tunnel coupling. If we assume that tunneling rates through the outer barriers, Γ_{BL} and Γ_{BR}, are equal and remain roughly constant in the three coupling regimes (these rates do change somewhat as indicated by a varying value of peak conductance in Fig. 7.3d, and limiting the validity of the following analysis) we can relate the tunneling rates to the typical peak current for the single dot case as $I_P \sim 80$ pA $= (4V_E e/k_B T)(\Gamma_{BL}\Gamma_{BR}/\Gamma_{BL} + \Gamma_{BR})$ to find $\Gamma_{BL} = \Gamma_{BR} = \Gamma \sim 9$ GHz, where V_E is the excitation voltage used in the measurement, and $T = 1.5$ K the measurement temperature (this formulation holds approximately for the conditions met in this case, $h\Gamma < k_B T$) [16]. Using these values we solve for the middle barrier tunnel rate, GM, from the peak current in the intermediate ($I_P \sim 60$ pA) and weak ($I_P \sim 10$ pA) coupling cases using $\Gamma_M^2 = I_P \Gamma^2 / 4(2e\Gamma - 3I_P)$ for the case of resonant tunneling (This expression is derived from eq. 15 of ref. [154], assuming current is allowed to flow in either direction through the dot, and zero detuning between the dots.). We find that for the intermediate coupling $\Gamma_M \sim 700$ MHz , and for the weak coupling case $\Gamma_M \sim$

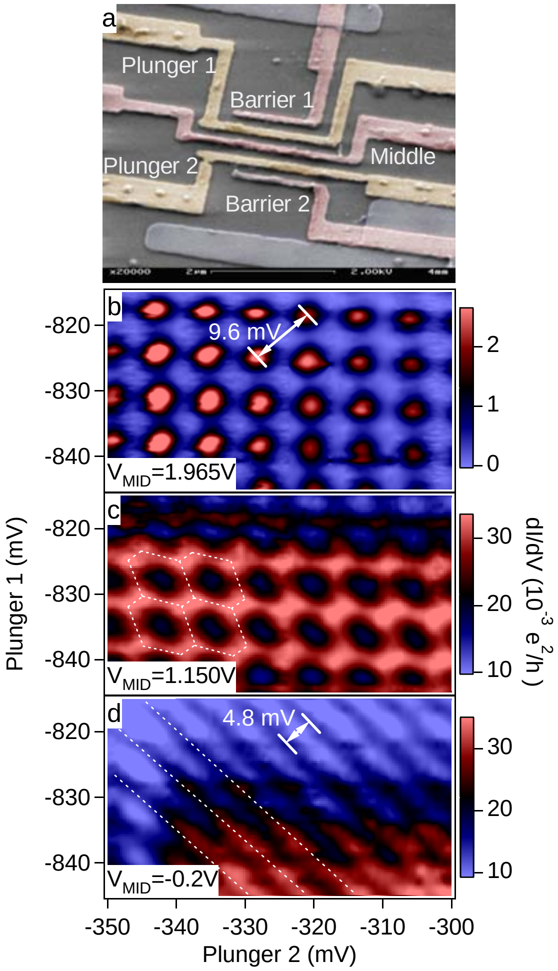

Figure 7.3: a) Colored SEM image of a five-gate carbon nanotube device lithographically similar to that measured. Pd contacts are visible at the top and bottom, under the SiO_2 insulator. The nanotube itself is not visible. Gates used to form dots are colored red while plunger gates which tune dot energy levels are colored yellow. Scale bar = 2 μm. b) dI/dV (colorscale) as a function of two plunger gate voltages. Barrier 1 = 389 mV, Barrier 2 = 1077 mV, Middle Gate voltage is indicated on the figure. Temperature = 1.5 K, ac excitation = 53 μV. For weak interdot coupling, high-conductance points appear on a regular array corresponding to resonant alignment of energy levels between the two dots with the Fermi levels of the leads. Note the low overall conductance. c) At intermediate interdot coupling (for lower middle gate voltage), cross-capacitance and tunneling between dots splits the degeneracy points, giving the familiar hexagonal double-dot charging diagram (dashed lines). Dotted while lines serve as guides to the eye. d) For strong coupling of the double dot (lowest middle gate voltage) the two plunger gates together on a single effective dot, producing single-dot charge states separated by diagonal stripes (dashed lines). Note the factor ~ 2 change in peak period between (b) and (d)

200 MHz, consistent with a modest visible splitting of the vertices for intermediate coupling. Finally, if we assume that in the weak coupling case tunneling through the middle barrier provides the dominant component of resistance, setting $\Gamma_M = I_P/e$ gives $\Gamma_M \sim 60$ MHz, smaller than, but comparable to the value of 200 MHz obtained above.

7.4 Comparison of devices using PECVD SiO_2 and ALD Al_2O_3

The data in Fig. 7.2c show significant off-resonance tunneling outside of the Coulomb diamonds, obscuring any excited state features that would be expected in low-temperature transport. We find that this washing out of excited state features is characteristic of devices made with PECVD SiO_2 but is typically not the case for ALD Al_2O_3, where excited state features are generally visible outside the Coulomb diamonds. We do not know if this difference is due to the oxide material itself or due to damage that occurs during deposition.

7.4.1 Single dots using ALD Al_2O_3

Figure 7.4 shows a series of Coulomb diamonds measured on a gate-defined quantum dot using ALD Al_2O_3 as an insulating layer. Off-resonance conductance is low, and excited states are visible outside of the boundaries of the diamonds. The mean level spacing extracted from the data $\sim$ 2–3 mV gives a measure of dot length, $L \sim$ 0.5–0.8 μm, again roughly consistent with the lithographic dimensions of the gated

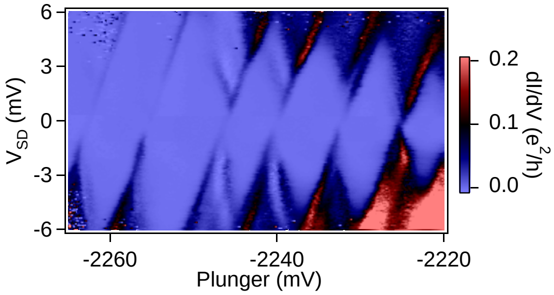

Figure 7.4: Coulomb diamonds measured on a device using ALD Al_2O_3 as the gate dielectric for $T \sim 270$ mK. Excited states are visible outside of the diamonds as off-resonance conduction is suppressed. Gates were ~ 150 nm wide with ~ 150 nm spacing. Barrier 1(2) = -993 (-2337) mV, Backgate = +16 V. This device is ambipolar, and here operated in the electron-doped regime.

region of the tube for this device.

7.4.2 Double dots using ALD Al_2O_3

The gate-controlled transition from open conduction to the Coulomb blockade regime has been investigated in eight devices with various gate dimensions, configurations, and dot sizes. Double quantum dot devices have been investigated using both SiO_2 and ALD Al_2O_3. Again, off-resonant conduction is reduced in double dots fabricated with ALD Al_2O_3 as a gate oxide compared to those using SiO_2. In addition, structure is visible inside the honeycomb vertex triangles for Al_2O_3 devices when measured at finite V_{SD} (see Fig. 7.5). A full understanding of these features requires further study.

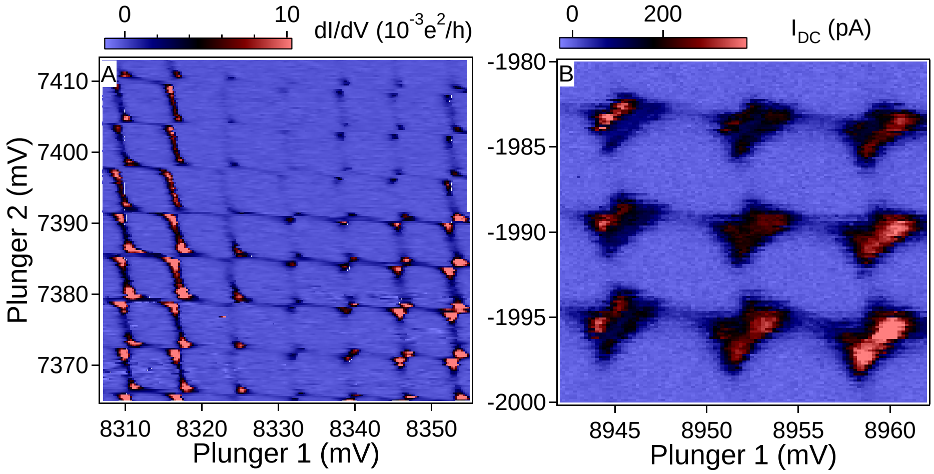

Figure 7.5: a) Honeycomb charge stability diagram (dI/dV, colorscale) for a gate-defined double dot using ALD Al_2O_3 as a gate insulator. $T \sim 270$ mK. Note the low off-resonance conduction and well isolated honeycomb vertices. b) I_{DC} for the same device measured at $V_{SD} = 1.5$ mV. Honeycomb vertices expand into finite bias triangles and show internal structure. Similar measurements of dI/dV for this region of gate voltage shows negative differential resistance

7.5 Conclusion and acknowledgements

We note that while nanotube double quantum dots have been previously investigated [111], and showed behavior comparable to the present results, this work differs from previous work in not relying upon intrinsic defects or tunnel barriers at the metal nanotube interface, instead defining quantum dots only using electrostatic gates. Controlled gating at arbitrary points along the tube greatly enhances the functionality of nanotube devices for potential applications ranging from bucket-brigade devices to quantum coherent logic elements. This approach may be particularly useful for quantum logic, as recent theoretical work has shown that a one-dimensional array of coupled quantum dots can be used for quantum computation [105, 31]. Further, the expected long spin coherence lifetime [53] for electrons and holes in nanotubes makes this an attractive material for developing spin-based quantum information storage and processing systems.

This work was supported by ARO/ARDA (DAAD19-02-1-0039 and -0191), NSF-NIRT (EIA-0210736), and the Harvard Center for Nanoscale Systems. M.J.B. acknowledges support from an NSF Graduate Research Fellowship and an ARO-QCGR Fellowship. S. G. acknowledges support from Bourse de Recherche, Swiss National Science Foundation. N. M. acknowledges support from the Harvard Society of Fellows.

Chapter 8

RF-reflectometry and capacitive charge detection

In this chapter I will introduce the techniques of capacitive charge detection and rf-reflectometry for the *fast* detection of single electron charging events. The first section of this chapter provides some of the necessary background material for a full understanding of the experimental section to follow. That section describes a set of experiments performed at the University of New South Wales in Sydney, Australia during a 2-month stay in the winter (in the northern hemisphere) of 2005. The results describe the incorporation of Al rf-SETs into gate-defined carbon nanotube quantum dot devices, representing an exciting combination of existing technologies to produce a novel readout technique for carbon nanotube devices.

8.1 Background

In the first section of this chapter I will introduce a number of techniques useful for the electrical detection of single electron charging *without* the use of direct transport measurements. These techniques are particularly useful from the perspective of quantum computation, where a noninvasive readout scheme is necessary.

8.1.1 Capacitive charge detection

The nonlinearity of the gate voltage response of a transistor allows these solid-state devices to be employed as amplifiers — a small input signal (applied to the gate) can dramatically change the device channel conductance, hence amplifying the input signal. Such devices have generally been employed in a digital fashion where the input signal simply switches the device from subthreshold to high conductance operation, forming the basis of digital switching for applications in logic gates.

A similar technique may be used in an analog fashion in order to amplify very small electrostatic potential changes associated with the rearrangement of charge in a nanoscale device. This is accomplished through the exploitation of nonlinearities in the gate response of a nanoscale conductor which is coupled capacitively to the system of interest. Past experiments have demonstrated the efficacy of charge sensing using quantum point contacts in GaAs heterostructures coupled to gate-defined quantum dots [46], but we will limit our discussion to the use of a single electron transistor as the sensing device.

We may model our circuit as in Fig. 8.1a, with an SET capacitively coupled to an environmental potential. In practice, this potential is generally derived from a

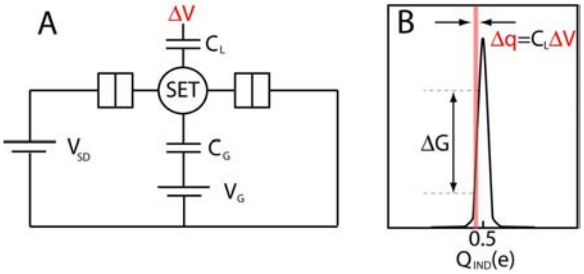

Figure 8.1: A) Circuit diagram for an SET (detector) capacitively coupled through C_L to an environmental potential (or device) which fluctuates in time, ΔV. B) This induces a charge $\Delta q \ll e$ on the SET island, which functions as an external gate voltage. If the SET is biased to the sidewall of a Coulomb blockade peak, a small change in induced charge produces a large measurable change in SET conductance, ΔG. Figure after [28].

device which we intend to address with the SET, such as a quantum dot. In this case, the addition of an electron to the quantum dot produces a potential change ΔV at the SET detector. Due to the capacitive coupling, this results in an induced charge on the SET which functions as an effective gate voltage (Fig. 8.1b). If the SET is biased with an external V_G to sit on the side of a Coulomb blockade peak, a small change in the effective gate voltage will produce a large change in SET conductance. Accordingly, a small potential change resulting in an induced charge $\Delta q \ll e$ may translate to a significant change in SET conductance, ΔG, which is easily measured using standard lock-in techniques.

8.1.2 The superconducting Al-SET

The detector employed in this work is the superconducting Aluminum SET. Although the physics of single electron charging is important in these devices, the fact that both the SET island and its leads are superconducting adds significant richness to the physics explored in a 2D plot of conductance as a function of V_{SD} and V_G. The device is operated in a regime such that the Josephson coupling energy, E_J, across the tunnel barriers separating the island from source and drain [85] is much smaller than the charging energy E_C of the island, making the number of Cooper pairs [13, 14] on the island well-defined.

Low-bias transport in the superconducting SET is dominated by the superconducting gap, Δ_S, such that for biases $V_{SD} < 4\Delta_S/e$ quasiparticle transport is suppressed. Beyond this threshold, single electron charging effects are visible, producing a diamond-like pattern in the 2D conductance plots. This causes the threshold of conductance to vary between $[4\Delta_S/e, 4\Delta_S/e + 2E_C]$ (Fig. 8.2). In the sub-gap region transport may only occur through two-electron or Cooper pair transfer processes. Among others, these include resonant cooper pair tunneling [73] and the Josephson quasiparticle (JQP) [59, 120, 152] and double Josephson quasiparticle (DJQP) [67] cycles . These higher order processes involving coherent, cyclical addition of cooper pairs and quasiparticles to the SET island appear in transport measurements such as those in Fig. 8.2. A more complete description of these processes may be found in [28].

We exploit the nonlinearities of the Al-SET transport characteristics to perform capacitive charge detection as described in Sec. 8.1.1. By appropriately biasing the Al-SET (applying V_{SD}) we may sit at the JQP point, DJQP point, or threshold of conductance, using either cooper pair resonances or single electron Coulomb blockade peaks to provide the necessary transconductance nonlinearity. One advantage of the superconducting SET over the normal SET is that the device differential resistance may be lower than the sum of tunnel junction resistances [8], providing the super-

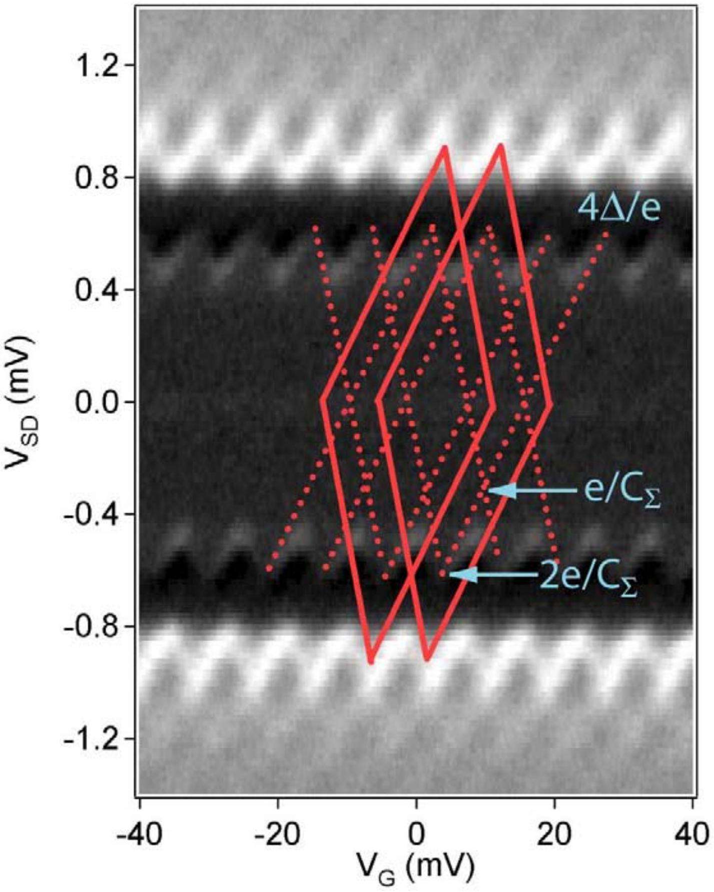

Figure 8.2: Conductance measured as a function of V_{SD} and V_G for a superconducting Al SET. White corresponds to device resistance $\sim$ 50 kΩ, dark to $>$ 100 M Ω. Measurements performed using rf-reflectometry (see Sec. 8.1.3). Solid lines indicate stability diamonds for fixed cooper pair numbers on the SET island. Dashed lines indicate energy conditions where resonant cooper tunneling may take place. The quasiparticle current threshold is noted at $4\Delta/e$ and the JQP and DJQP energies are indicated on the figure as $2e/C_\Sigma$ and e/C_Σ respectively, coinciding with measured sub-gap features.

conducting SET with a larger dynamic range than its normal cousin. Calculations show that the sensitivity of a superconducting SET approaches $2\mu e/\sqrt{Hz}$, in principle allowing for the detection of $2\mu e$ with an integration time of 1 s under ideal conditions.

8.1.3 RF-reflectometry

Measurements of changes in SET conductance are limited to a frequency $f_{max} = (2\pi RC_{Lead})^{-1}$ where R is the SET resistance and $C_{Lead} \sim 1$ nF is the parasitic capacitance of the lead wires running down the cryostat. For a standard Al-SET with $R \sim 50$ kΩ, this imposes a bandwidth limit of $f_{max} \sim$ 3kHz. By comparison, the intrinsic RC cutoff frequency for a device with total capacitance of order aF may be greater than 10 GHz. An approach designed to overcome the effect of this parasitic capacitance was developed by Schoelkopf *et. al* [141]. There, an impedance matching network was employed to transform the device resistance to the characteristic impedance (50 Ω) of a radio-frequency (rf) network. Changes in device resistance were detected by measuring the damping of a reflected rf signal applied to the device at the resonant frequency of the impedance matching circuit, permitting measurements with a bandwidth of $>$ 100 MHz, limited instead by the Q-factor of the impedance matching network.

Impedance matching networks

Standard rf transmission lines have a characteristic impedance $Z_0 = 50\ \Omega$, leading to a large reflected voltage signal when connected to a load with a characteristic impedance, Z_{load}, differing from 50 Ω. The amount of reflected signal for a given (time-oscillating) V_{in} is given by the coefficient $\Gamma_R = V_{out}/V_{in} = (Z_{load} - Z_0)/(Z_{load} + Z_0)$, which changes little for $Z_{load} \gg Z_0$ in the case of an SET whose resistance varyies between 50 kΩ and $\sim$ GΩ. Accordingly it is customary to incorporate the device load into an LCR resonant circuit whose characteristic impedance, $Z_{LCR} \sim Z_0$ on resonance. For the resonant or "tank" circuit shown in Fig. 8.3b (L in series with C and R in parallel) it can be shown [28] that

$$Z_{LCR} = \frac{R}{1 + \omega^2 C^2 R^2} + i\frac{\omega L - \omega C R^2 (1 - \omega^2 LC)}{1 + \omega^2 C^2 R^2} \tag{8.1}$$

On resonance the stored magnetic energy in the inductor is equal to the stored electric energy in the capacitor, and the reactive components of Z_{LCR} vanish, allowing calculation of ω_{res}. At this frequency $Z_{LCR} = L/RC$, and we may simplify the expression for the resonant frequency to $\omega_{res} = \sqrt{1/LC}$ if we wish to transform $Z_{LCR} \rightarrow Z_0$. Thus, by construction, on resonance we transform the impedance of the LCR circuit to the characteristic impedance of the transmission line. Any change in R (the device) will shift Γ_R from $0 \rightarrow 1$. It is useful to express this condition in terms of the reflected (P_{ref}) and incident (P_{in}) rf *power* using [28]

$$P_{ref} = P_{in}\left(1 - 4Q^2 \frac{Z_0}{R}\right) \tag{8.2}$$

$$Q = \left(\frac{\sqrt{L/C}}{R} + \frac{Z_0}{\sqrt{L/C}}\right)^{-1} \tag{8.3}$$

where Q is the loaded quality factor of the LCR circuit. From equation 8.2 it is obvious that a change in device resistance, R, will produce a change in the reflected rf power. In practice this is accomplished using a network analyzer or signal source tuned to the resonance frequency to output rf power and measuring the reflected rf signal after cryogenic and room-temperature amplification. (For a further discussion of experimental details please see section 8.2). A representative trace of reflected rf power for different values of device R embedded in an LCR circuit is shown in Fig. 8.3c.

Homodyne detection and wavelength division multiplexing

Changes in P_{ref} may be measured in real time using homodyne detection. In this technique, rf-power reflected from the tank circuit is mixed with a reference signal at the same frequency. Changes in the reflected signal from the demodulation circuit are detectable as an intermediate frequency (IF) voltage output from a standard microwave mixer (the 2f component is filtered out). Such changes are detectable on time scales falling within the bandwidth of the resonant tank circuit, which is often in excess of 100 MHz.

One may extend this technique to incorporate multiple tank circuits with different resonant frequencies connected to a single coaxial line using a technique adopted from telecommunications called wavelength division multiplexing. In the approach applied in the experimental section of this chapter to follow, two incident carrier wave signals are passed through directional couplers held at room temperature. Here -16 dB is directed toward the two tank circuits at each frequency, and both signals are combined onto a single coax entering the cryostat (Fig. 8.3b). The remaining -0.11 dB of each signal is directed to room temperature mixers. The rf power sent down the cryostat passes through another directional coupler mounted on a cryogenic stage of a dilution refrigerator and is coupled to the tank circuits. Reflected power passes through a cryogenic amplifier (+40 dB) and a room temperature amplifier (+45 dB) before being split and mixed with the reference signals for demodulation. The output of the demodulation circuit (after appropriate filtering) is a time varying voltage proportional to the reflected rf-power and is measured using an oscilloscope for time domain measurements.

8.2 Single charge detection in carbon nanotube quantum dots on microsecond timescales

8.2.1 Introduction

Carbon nanotubes are promising systems on which to base the development of coherent electronic devices [115, 102, 22]. Owing to a combination of their large energy level separations and quantized phonon spectrum [158], and together with an absence of nuclear spin moments, carbon nanotubes are likely to exhibit long-lived coherent states commensurate with other carbon-based systems [53]. Key to the success of this technology are both the ability to manipulate and couple coherent electron states within a nanotube and to perform readout with an efficiency that approaches quantum limits. In light of these sentiments, recent advances [22, 82, 81, 20] have enhanced the functionality of carbon nanotube devices towards the control of coherent electronic states, allowing the creation of multiple quantum dots along the length of a tube with controllable coupling solely by applying voltage biases to electrostatic top-gates [19]. Conversely, the readout of such novel structures has been limited by a reliance upon dc transport measurements, which although successful in uncovering their transport properties, are highly invasive and generally slow in comparison to the expected relaxation times of these systems.

In this Letter we describe the integration of superconducting aluminum radio frequency single electron transistors (rf-SET) [141] with carbon nanotube intra-tube quantum dot devices defined by electrostatic gates [19]. The rf-SET serves as an extremely sensitive electrometer [45] and when capacitively coupled to the nanotube dot, provides a means of non-invasively detecting its charge state on fast time-scales and in regimes that are not accessible with transport measurements [46, 106, 30, 157, 51]. In addition, we make use of a radio-frequency (rf) reflectometry technique that enables fast transport measurements of the nanotube in correlation with the fast charge sensing associated with the capacitively coupled rf-SET.

8.2.2 Methods

Nanotube device fabrication

Carbon nanotubes were grown from patterned Fe catalyst islands on a Si/SiO$_2$ wafer via chemical vapor deposition using methane as a carbon feed-stock. Single-walled tubes were located using atomic force microscopy and tubes with diameters less than ∼4 nm were selectively contacted via electron beam lithography [22]. Contacts were metallized with ∼15nm of Pd [81] and connected to metal pads defined by optical lithography. The entire device was coated with ∼35nm Al$_2$O$_3$ using a low-temperature atomic layer deposition (ALD) process. Three top-gates were then aligned to each nanotube; two barrier gates to deplete the underlying nanotube, defining a quantum dot, with a third plunger gate between these to tune the energy levels of that dot (Fig. 8.3a) [19]. The doped Si wafer also serves as a global back-gate. Metallic nanotubes which showed little gate response were excluded from the present study. The capacitive coupling between the SET 'island' and the nanotube dot was enhanced with the use of a 50nm Ti/AuPd (20/30) metal 'antenna' that crosses the tube and sits under the SET island. Subsequently, using a bilayer resist and double-angle evaporation technique [58] an aluminum SET was fabricated on the base of the coupling antenna (see Sec. 8.2.2 and Fig 8.3a).

SET Fabrication

The Aluminum SET is fabricated using a bilayer resist mask with an undercut in order to perform shadow-mask evaporation. The bottom resist layer is AR-P 619.08 Copolymer spun on at 6700 RPM for 60 s. Following a 10 min hotplate bake at 180 C, the sample undergoes a UV exposure for 30 min. 2.2 M PMMA is then spun on at 2400 RPM for 60 s, again followed by a 20 min hotplate bake at 160 C. Aluminum evaporation is performed in a system with an oxidation chamber and an electrically controlled rotating/tilting stage. For the first evaporation step, a 35 nm layer of Al forming the SET island is deposited at an evaporation angle of 12.5 degrees (from horizontal). The Al is oxidized at 35 mTorr for 10 min to form an oxide layer $\sim$ 1 nm thick, with a calibrated resistance $\sim$ 25 kΩ. The chamber is pumped to base pressure, the stage rotated 180 degrees and the second deposition of 38 nm completed.

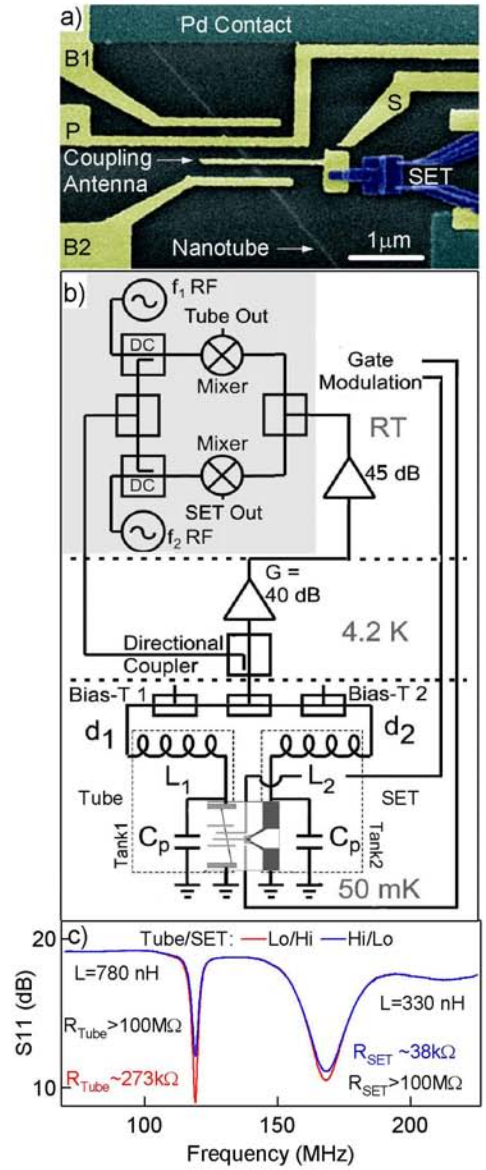

Figure 8.3: a) False-color SEM image of a representative quantum dot device with integrated Al-SET. The nanotube is visible under ALD Al_2O_3 and the Pd contact (top). Gates (yellow) are labeled on the figure. The Al-SET (blue) is aligned to a coupling antenna running over the nanotube. b) Schematic of the measurement setup for the multiplexed rf-reflectometry. c) Reflected rf signal as measured with a network analyzer for different values of nanotube and SET resistances. In this trace, the nanotube resistance is controlled with the back-gate while that of the SET is changed by shifting the bias voltage in or out of the superconducting gap.

RF circuitry

Devices were mounted on a circuit board engineered with rf coplanar waveguides and cooled in a dilution refrigerator with a base temperature of 30-50mK. Electron temperatures as measured in similar configurations are 100-200mK. Figure 8.3b is a schematic of our setup, showing the generation of the reflectometry 'carrier' signals at frequencies f_1 and f_2. These two carrier signals are combined and fed to a directional coupler housed at 4K within our dilution refrigerator. Two tank circuits transform the high resistance of the SET (~ 50 kΩ) or nanotube (~ 200 kΩ) towards $\sim 50\Omega$, at the resonance frequency $f_{1,2}$ set by the parasitic capacitance C_p and chosen series chip-inductor ($L = 780$ nH for the nanotube and $L = 330$ nH for the SET). At resonance, changes in resistance of either the nanotube or SET are mapped to changes in the amount of reflected rf-power. After amplification at 4 K (40 dB) and room temperature (45 dB) the signals are demodulated using a homodyne technique to produce an output voltage proportional to the change in device resistance. Wavelength division multiplexing enables simultaneous monitoring of both devices, which operate at different frequencies but utilize a common transmission line and cryogenic amplifier [142, 29].

Tank circuit and SET calibration

Figure 8.3c shows the amount of reflected power from the tank circuits as a function of frequency measured with a network analyzer after amplification. The two resonances are easily identified at $f_1 \sim$120MHz for the nanotube and $f_2 \sim = 165$ MHz for the SET. Estimating the bandwidth from these measurements suggests ~ 1 MHz for the nanotube and ~ 10 MHz for the SET. We note that the use of rf-reflectometry in order to measure changes in resistance of a nanotube has been performed previously [101], but only for slow measurements in field effect transistor device configurations. Bias-tees, comprising of surface mount components on the circuit board, facilitate standard low-frequency lock-in resistance measurements and voltage biasing of both the SET and nanotube.

Figure. 8.4a shows a diamond charge stability plot for a representative superconducting SET (used for all measurements in Fig. 8.4). We plot the demodulated voltage signal as a function of both the dc source-drain bias V_{SD}^{SET} across the SET and the voltage applied to a nearby gate electrode. We typically bias the SET using a battery box at the threshold of quasi-particle transport, $V_{SD}^{SET} \sim 4\Delta/e$, where the rf-SET sensitivity is maximized. Charge sensitivities for the two SETs used in this study are better than $\delta q = 10^{-5} e/\sqrt{Hz}$.

8.2.3 Charge detection in gate-defined nanotube quantum dots

We form a quantum dot in the carbon nanotube by applying appropriate negative voltages to gates B1 and B2 (Fig. 8.3a) with the back-gate set such that the device is n-type. The section of the nanotube between depletion regions formed in the tube by gates B1 and B2 serves as the quantum dot. In this configuration, Coulomb blockade (CB) is observed in standard lock-in transport measurements, manifested as a series of peaks in conductance as a function of a gate voltage (here, the P-gate) which is capacitively coupled to the dot [19] (Fig. 8.4b). The gate induces an effective charge on the dot (q_{ind}), and when $q_{ind} = e/2$ the n and $n+1$ charge states on the dot become degenerate and transport is allowed (similar physics is responsible for operation of the SET electrometer).

In the fast reflectometry configuration, a triangle wave voltage ramp is applied to the P-gate which moves the device through CB, and a compensating gate ramp is applied to the S-gate to maintain the SET at a fixed conductance value. When the P- and S-gates move together in the same direction, the SET is uncompensated and exhibits Coulomb blockade. In the region where P- and S-gates move in opposite directions the SET is compensated.

We exploit the large transconductance of the SET to perform sensitive electrometry measurements, as charge fluctuations in the nanotube quantum dot move the SET conductance up or down the side of a conductance peak. As we sweep the P-gate in the compensated configuration, the SET exhibits a characteristic sawtooth charging pattern on sub-millisecond time scales (Fig. 8.4c) [64]. The sawtooth slope is associated with gate-induced charging of the nanotube dot (which is coupled to the SET), followed by the tunneling of an electron onto the dot at the condition for charge degeneracy described above. The period of the sawtooth in plunger gate voltage is nearly identical to that measured directly from lock-in transport measurements of Coulomb blockade in the nanotube. By contrast, if the barrier gate voltages are now set such that there is no dot formed in the tube, we observe a nearly smooth line in the SET response (black trace, Fig. 8.4c). This indicates that the observed sawtooth response corresponds to charging of the *gate defined* nanotube quantum dot and not spurious charge traps. We note that the magnitude of the charge induced on the SET with the addition of a single electron to the nanotube dot is $Q_{SET} \sim e/4$, indicating strong coupling between the nanotube and the SET electrometer.

8.2.4 Nanotube stability diagrams measured via charge sensing

Similar measurements demonstrate the utility of charge sensing to map full charge stability diagrams, and reveal information not generally observable through transport measurements. Plotting the (compensated) SET signal as a function of time (P-gate voltage) and V_{SD} on the tube reveals a familiar diamond pattern associated with Coulomb blockade (Fig. 8.5a). For these measurements the applied V_{SD} on the nanotube couples capacitively to the SET itself and is compensated by adding a dc offset to the gate ramp. The nanotube quantum dot charge configuration is fixed in the diamond regions (and current blocked), while the blockade is lifted and current flow allowed at sufficiently high values of V_{SD}. In appropriate configurations of gates B1 and B2, we observe even-odd filling in the nanotube quantum dot [38], indicated by an alternating pattern of large and small diamonds. This is consistent with a shell-filling model in which a single electron can enter a discrete energy level in the dot with charging energy $E_C = e^2/C$ and quantum level spacing ΔE. The second electron, with opposite spin to the first can enter the same orbital state requiring only E_C. Estimating ΔE for a dot of the size used in this experiment to be $\Delta E = 750\mu V$ using $\Delta E = hv_F/2L$, where $L \sim 1\mu$ m is the dot length, consistent with experimental measurements. In this particular gate configuration we do not observe four-fold shell filling [103, 140], although it has been observed in this device using standard lock-in

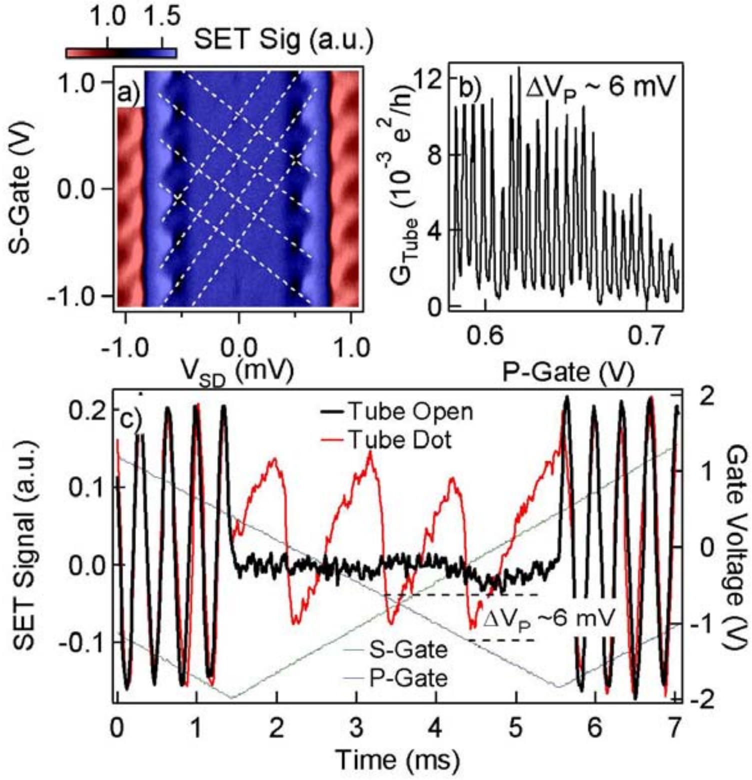

Figure 8.4: a) Charge stability diamonds for a superconducting rf-SET. We plot the demodulated voltage signal from our homodyne detection circuit. For the intensity scale red corresponds to $\sim$ 50kΩ and blue $\sim$ 100MΩ. Dotted lines indicate conditions for resonant cooper-pair tunneling. b) Coulomb blockade in the nanotube as measured using standard lock-in techniques with gates B1 and B2 near 2V, BG=18V, V_{SD}=1.5mV. c) rf-SET signal (averaged 60 times, left axis) in the time domain (arb. offset) with the SET biased to a sensitive region. Green and blue traces indicate triangle wave gate ramps for S- and P-gates (with -40dB of attenuation) respectively (right axis). When no dot is formed in the nanotube (B1=B2=10V) we observe a flat line in the rf-SET response, while forming a dot as in panel b) yields a sawtooth charge sensing signal.

measurements.

In addition to the low-bias diamonds visible in transport, for particular configurations of gate bias, we are also able to map out Coulomb diamonds beyond the first order and detect the *Coulomb staircase* in V_{SD}. This is most likely possible because the SET senses the time averaged charge on the nanotube dot and not the current that flows from source to drain, which in transport measurements is affected by co-tunneling processes at high V_{SD}. We observe diamonds centered at $V_{SD} = e/C_{\Sigma}$, the bias corresponding to the apex of the first order classical diamonds, where C_{Σ} is the capacitance of the dot. First, second, and the beginning of third order diamonds are visible in Fig. 8.5b, each offset by e/C_{Σ} from the center of the diamonds of the next lower or higher order. We have also seen indications of Coulomb diamonds in the charge sensing signal to the fourth order, although in some cases we do not see higher order diamonds at all (e.g. Fig. 8.5a). These differences are presumably related to the variations in the symmetry of the tunnel barriers as defined by the top-gates.

8.2.5 Simultaneous multiplexed reflectometry measurements

As noted above, our multiplexing demodulation circuit permits fast simultaneous measurements of both the nanotube and SET. As such we are able to perform correlation measurements using the direct rf-transport signal from the tube and the non-invasive signal from the rf-SET electrometer. Figure 8.6a shows both the demodulated signal from the nanotube tank circuit as well as that from the SET for S- and P-gate ramps with the nanotube in the CB regime (different device). CB peaks are evident in the reflected signal from the tube, and a sawtooth pattern is visible in

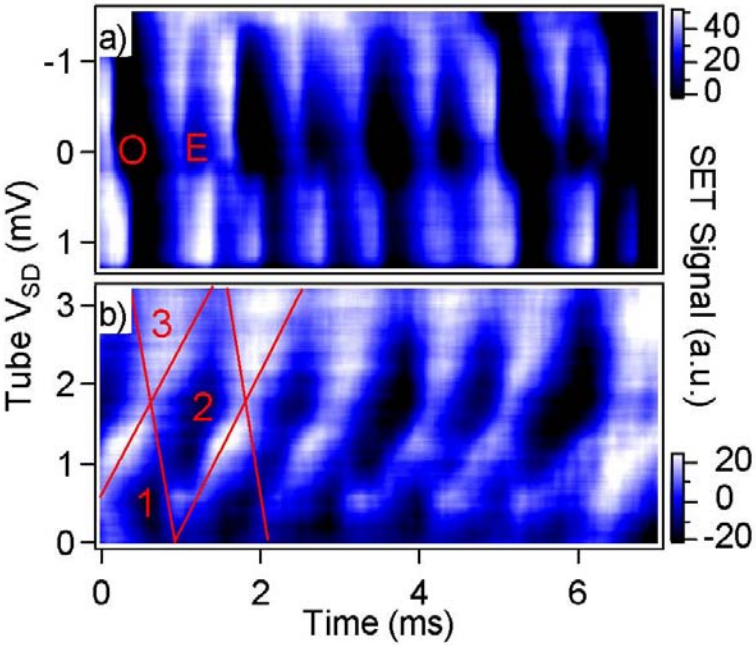

Figure 8.5: a) SET signal as a function of time (P-gate) and V_{SD} across the nanotube showing even (E) and odd (O) filling of energy states in the nanotube quantum dot. b) Similar measurements in a different configuration of B1 and B2 showing first, second and third order Coulomb diamonds with increasing V_{SD}. Red lines are guides to the eye indicating the boundaries of diamonds in which charge number on the dot is fixed.

the SET signal, with sequential charge addition occurring on time scales of $\sim 300\mu s$ (we have performed similar measurements with charge addition periods $\sim 30\mu s$, but systematic noise increased with gate speed). The two signals are correlated as expected, with the apex of each Coulomb blockade peak falling roughly in the middle of the charging sawtooth. Further, the width of the transition region for each sawtooth charging event is roughly equivalent in time to the width of the Coulomb blockade peak.

Extending these measurements, we construct charge stability plots for the nanotube quantum dot by simultaneously measuring the (demodulated) SET (Fig. 8.6b) and tube signals (Fig. 8.6a) as a function of V_{SD} across the nanotube. We again measure charge stability diamond plots, observing nearly identical Coulomb diamonds from both the nanotube and SET signals. The SET, however, is sensitive to charge fluctuations in regions of V_{SD} and P-gate voltage where direct transport measurements do not yield measurable currents, and where resistance changes in the nanotube mapped through reflected-rf are immeasurable.

8.2.6 SET backaction

We have also studied how the V_{SD}^{SET} biasing point of the SET influences the Coulomb blockade in the nanotube quantum dot. Consistent with measurements made on Aluminium single-electron boxes [150], we observe asymmetries and changes in the width of the CB peaks with varying V_{SD}^{SET} across the SET (Inset Fig. 8.6a). This behavior is likely due to a convolution of heating [96] and the backaction connected with charge fluctuations of the SET island as current flows from source to drain. Of

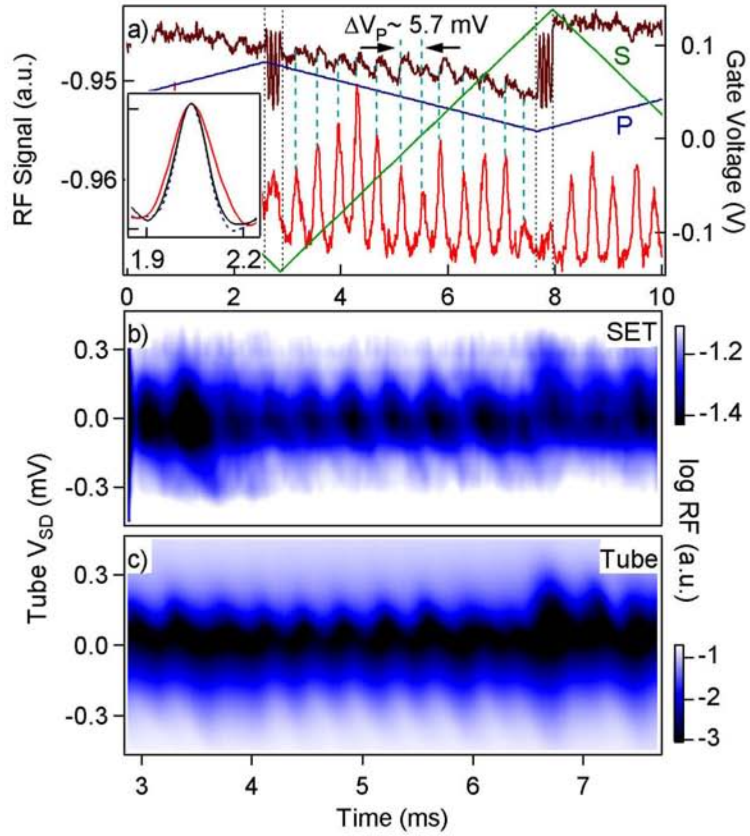

Figure 8.6: a) Fast, simultaneous measurement of the rf-SET and nanotube using rf-reflectometry at tube $V_{SD} \sim 250\mu V$. Coulomb blockade peaks are evident in the nanotube signal (red lower trace) corresponding to a sawtooth in the SET signal (CB is evident in the SET signal at points where the gate biases change sweep direction). For this device gate B2 was shorted to the tube source and hence held at V=0. B1=0V, BG=7.78mV. **Inset:** (lower left corner) shows the backaction dependence of a CB peak in the tube as measured using reflectometry at different V_{SD}^{SET} for the SET. SET V_{SD}^{SET} biased to the gap (black trace), biased to the DJQP (blue and dashed trace) and $\sim 3mV$ (red trace). b)-c) Reflected rf signal on a logarithmic color-scale from the SET and tube respectively (gate ramps identical to those in panel a)) as a function of V_{SD} across the tube. Coulomb diamonds are visible in both panels, with key features reproduced between both. Each sweep at fixed V_{SD} has been averaged 1000 times.

particular interest, we see a slight *narrowing* of the Coulomb blockade peaks in the nanotube dot when the SET is biased near the double Josephson quasi-particle resonance (DJQP) [37], relative to the CB peak-width when the SET is biased into the superconducting gap. A full understanding of such effects requires further study in order to clearly characterize the backaction mechanisms in play.

8.2.7 Conclusions and acknowledgements

In conclusion, we have presented fast rf-reflectometry measurements of a gate defined quantum dot in a carbon nanotube. With the incorporation of Al rf-SETs we are able to perform non-invasive charge sensing measurements of the quantum dot on fast time-scales in correlation with fast reflectometry and standard dc transport measurements. Our results demonstrate the feasibility of this technology for fast and near quantum limited readout of nanotube based coherent electronic devices.

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Chapter 9

One-dimensional ballistic transport

In this chapter we introduce the concepts of transport in low-dimensional structures, ignoring zero-dimensional states previously discussed in Ch. 4. The first section of this chapter presents the concepts of ballistic transport and the Landauer formalism for transport in 1D systems. Experiments demonstrating these effects will also be discussed briefly. Subsequently, in section 9.2 we will proceed to discuss transport experiments on carbon nanotubes with local depletion regions. These measurements reveal characteristics of 1D ballistic transport and also present a surprising finding about conductance quantization in carbon nanotubes.

9.1 Transport in 1D

In any discussion of transport in low-dimensional structures, there are several length scales which must be defined in order to understand the physical phenomena in play. These are:

- The electron Fermi wavelength, λ_F
- The mean free path or momentum relaxation length, ℓ_m
- The phase coherence length, ℓ_ϕ, over which quantum mechanical phase information is retained.

In general, the dimensionality of a conductor is set by the magnitude of the Fermi wavelength: if the size, l, of a conductor in any dimension is much larger than λ_F, then the wave nature of the electron may be neglected in that dimension. In this manner it is possible to define a one-dimensional conductor as one in which $\lambda_F \sim l$ in two dimensions. (For the purpose of our discussion we will begin with a 2D electron system which we then confine laterally). Alternatively, one may say that with confinement in two dimensions, the density of states is comprised of 1D modes (also subbands) due to the quantization of the momentum wavevector in the transverse dimensions. In this manner one may write the number of 1D modes, $M \approx Int\left(\frac{W}{\lambda_F/2}\right)$, i.e. each mode must accommodate approximately half of a Fermi wavelength.

9.1.1 Ballistic transport in 1D

Under the conditions $l \ll \ell_m$ for a conducting channel of length l, transport is termed ballistic, indicating that it traverses the length of the channel without momentum relaxation. Ohmic scaling, which states $G = \sigma W/l$ with σ the material system's conductivity and W the channel width, suggests that as the channel length is reduced, total conductance should increase to infinity. Experiments, however, show that the conductance saturates at a fixed value. We now show that the saturating conductance is due to a contact resistance as electrons scatter from bulk leads into the narrow conductor where transport occurs via quantized 1D modes.

Classically one may write the current carried by a wire as $I = nev$ with n the electron density and v the electron velocity. This may be generalized, assuming periodic boundary conditions in 2D, by writing

$$I = 2 \times \frac{1}{2\pi} \int dk \, \nu e v \tag{9.1}$$

where the first factor of 2 is for spin degeneracy and ν is the electron density of states. One notes that the electron velocity, $v = \partial E/\partial k$, and the density of states $\nu = (1/\hbar)(\partial k/\partial E)$. Thus in the above integral the energy dependence of the integral vanishes and we are left with a total current $I = 2e/h$ per mode, which may be transformed to a conductance $G = 2e^2/h$ per mode.

Electrons are injected into 1D modes of the channel at the chemical potential of their respective source electrodes. The absence of scattering inside a ballistic channel produces no voltage drop along the channel length, and hence the chemical potentials for left and right movers are constant across the channel. Accordingly, all of the voltage drop associated with the quantization of conductance occurs at the leads such that we may defined a contact resistance of 12.9 kΩ per mode, consistent with experimental observations. With respect to a 2D conductor constricted to form a 1D channel, we see that conductance through the system increases stepwise as the number of modes is increased (each time the channel becomes wider by $\lambda_F/2$). This was observed first by van Wees and Wharam in simultaneous measurements [156, 164] (see Fig. 9.1).

In the case of a nanotube we note that there exists an additional degeneracy arising

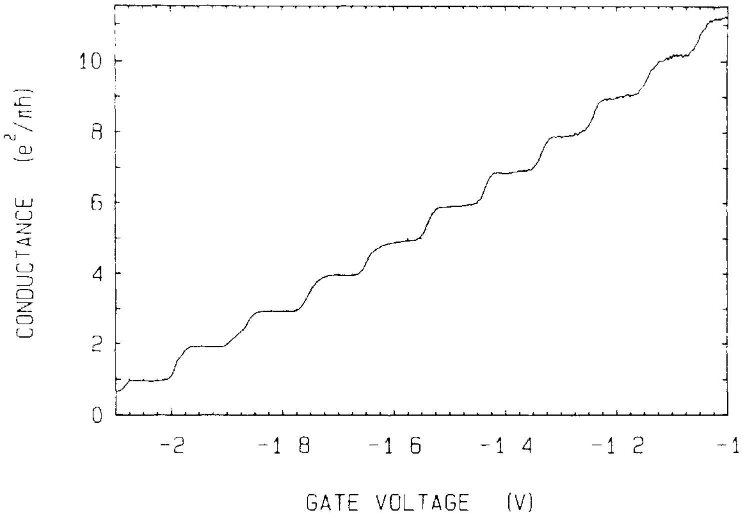

Figure 9.1: Conductance quantization in units of $2e^2/h$ from [156]

from the band structure of the nanotube. Hence, the total conductance, including band and spin degeneracies, through a 1D subband of the graphene sheet (only one allowed $\vec{k}_\perp$) should be $4e^2/h$. Further discussion will follow in section 9.2.

9.1.2 The influence of scattering

In the Landauer formalism we combine the conductance quantization derived above with a transmission probability, T, to write

$$G = \frac{2e^2}{h} MT \tag{9.2}$$

with M the total number of occupied modes. This allows the inclusion of scattering in the channel by considering a finite probability of electron reflection in the conductor. Note that this formulation neglects quantum interference effects (for one manifestation of such effects in a carbon nanotube see section 9.1.4).

For a system with two series scatterers, one may write the total transmission $T_{12} = T_1T_2/(1 - R_1R_2)$, considering multiple reflections [41]. This has a special additive property such that for N scatterers with fixed transmission probability T

$$\frac{1 - T(N)}{T(N)} = N\frac{1 - T}{T}. \tag{9.3}$$

Accordingly, the resistance of an individual scatterer is proportional to $(1 - T)/T$. For a linear density of scatterers, $N = \nu L$, we may write $T(L) = L_0/(L + L_0)$, with $L_0 = T/\nu(1-T)$, a length of order the mean free path. Hence one may write the total device resistance as the sum of the contact resistance and the scattering resistance as

$$R = \frac{h}{2e^2M}\frac{1}{T} = \frac{h}{2e^2M} + \frac{h}{2e^2M}\frac{1 - T}{T}. \tag{9.4}$$

Such a formulation also leads to the recovery of Ohm's law for a wide conductor with many modes [41].

9.1.3 The Tomonaga-Luttinger liquid

The whole of the discussion above was derived from a Fermi liquid picture of interacting electrons in a constriction. Although this description accurately predicts the quantization of conductance in narrow channels, it ignores several important qualifications. In 1D, nesting of the Fermi surface at $2k_F$ leads to the opening of a Peierls gap in the energy spectrum when the $\pm k_F$ states are coupled adiabatically by electron-electron interactions (or phonons). Accordingly, the states which are closest to the Fermi energy and hence quasi-stable eigenstates (quasiparticle lifetime in Fermi liquid theory, $\tau \sim (E - E_F)^{-2}$) vanish. In this sense, the quasiparticle excitations of the Fermi liquid no longer adequately describe the dynamics of the system. Instead, Tomonaga and Luttinger derived the low-energy dynamics of the system, and found the excitations could be modeled as exactly soluble collective bosonic modes [149, 107]. Their models show that the presence of electron-electron interactions in a 1D system renormalize various energy scalings and even the conductance quantum by a microscopically derived "Luttinger parameter." For a more formal and thorough treatment of the topic please see Refs. [68, 159].

We note that evidence of Luttinger liquid behavior has been observed in carbon nanotubes [24], although such effects are largely irrelevant to the work presented in this thesis. One exception is the presence of a power-law scaling in the density of states which produces a "zero-bias anomaly," $dI/dV \sim V^{\eta}$ with η derived from the Luttinger parameter in a carbon nanotube. This is manifested as a dip in the conductance of a metallic nanotube (or a nanotube doped such that it behaves as a metal) near zero V_{SD}, which scales as a power-law in temperature. The Luttinger parameter may be written [49, 87]

$$g = \left(1 + 2\frac{E_C}{\Delta}\right)^{-1/2} \tag{9.5}$$

which, using the previously derived values of the charging energy and level spacing, suggests $g \sim 0.28$ for a carbon nanotube.

9.1.4 Fabry-Perot interference

When the phase coherence length is the longest in the problem, quantum interference effects become important in the transport characteristics of a low-dimensional conductor. This is particularly true for carbon nanotubes, where electrons backscattered from partially reflecting nanotube-metal contacts interfere with themselves to

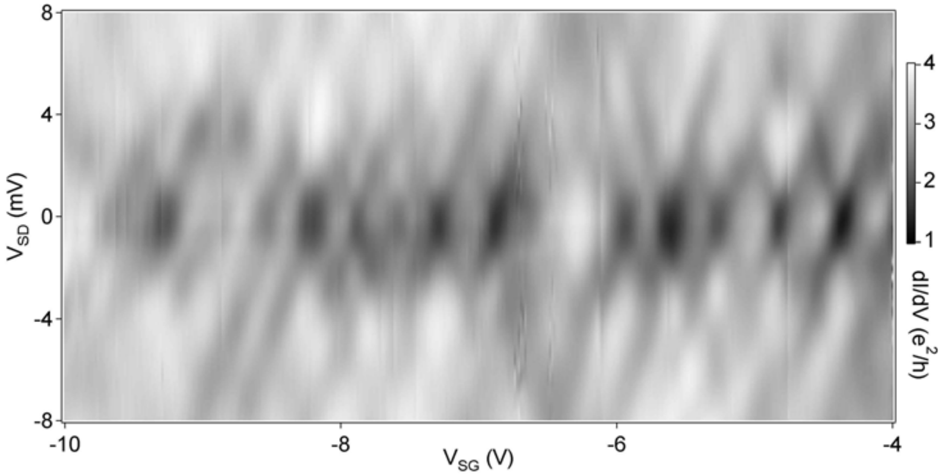

Figure 9.2: Fabry-Perot interference in a carbon nanotube measure at $T = 4$ K. Numerically differentiated from measured dc current. V_{SG} is a sidegate voltage applied to a mechanically deformed section of the nanotube.

produce Fabry-Perot resonances (in analogy to the optical cavity). This was first observed by Bockrath [102] in a metallic carbon nanotube with highly-transparent contacts, and a capacitively coupled gate electrode. In these (and other) measurements, a 2D plot of conductance as a function of V_G and V_{SD} produced an alternating pattern of high and low-conductance as in Fig. 9.2.

The origin of this conductance pattern may be derived by examining the effect of both dc bias and gate voltage. Shifting the bias across the tube changes the wavelength of the electrons at the chemical potential of the source electrode. The gate voltage, similarly, couples to the potential energy of the electrons, $\Phi_{eV}(x)$, where x is the position along the tube axis. The average potential, $\langle \Phi_{eV} \rangle$, may be related to the induced charge density on the tube and hence the gate voltage, after Bockrath, as $Q = LC_L V_G = \frac{-8Le}{hv_F} \langle \Phi_{eV} \rangle$.

We see that the electron wavevector shifts with applied gate voltage as $k(x) =$

$k_F \pm (E - \Phi_{eV}(x))/(\hbar v_F)$, with E the total electron energy. This wavevector may be integrated over the tube length to give a phase shift $\phi = k_F L \pm L(E - \Phi_{eV}(x))/(\hbar v_F)$. Using the relation above between the induced charge and the average potential we find

$$\phi_{1,2} = k_F L \pm \left(\frac{EL}{\hbar v_F} + \frac{\pi L C_L V_G}{4e} \right). \tag{9.6}$$

Here, the subscripts (1,2) denote the two degenerate modes in the nanotube subband. This phase shift enters into an intratube scattering matrix, which when combined with scattering vectors at the left and right leads [102] can be used to calculate the transmission and reflection coefficients for each mode in the nanotube. Interference between modes with different phases leads to the observed conductance pattern. As this relies upon phase-coherent transport, the appearance of Fabry-Perot interference fringes indicates that $\ell_{phi} \gg L$. The observed pattern becomes washed out with increasing V_{SD}, likely due to electron heating, and similarly fades with increasing measurement temperature. For an extended discussion of Fabry-Perot interference in nanotubes, see Sec. 9.2.5.

9.2 Anomalous conductance quantization in carbon nanotubes

9.2.1 Introduction

Carbon nanotubes free of disorder are expected to behave as ideal quantum wires with electrical conduction occurring through one-dimensional (1D) modes [4], each with conductance quantized in units of e^2/h. In a variety of physical systems, including gate-defined quantum point contacts [156] and cleaved-edge wires [169], such 1D behavior appears as conductance plateaus as a function of voltage on nearby gates, which act to reduce density in the wire and hence depopulate 1D modes. In gated heterostructure quantum point contacts, conductance steps of $2e^2/h$ are observed, the factor of 2 reflecting spin degeneracy of the subbands [155, 17]. By analogy, one would expect nanotubes to show either a single step of $4e^2/h$, reflecting the four modes per subband associated with spin and band degeneracy [3, 103], or two steps spaced by $2e^2/h$ if band degeneracy were lifted, for instance by strain [103]. In this section we report conductance plateaus in gated nanotube devices in various configurations, revealing an unexpected plateau spacing of $1e^2/h$ at zero applied magnetic field.

Conductance quantization has previously been observed in multiwalled carbon nanotubes by immersing one end in a liquid conductor [54]. This study found quantization principally in units of $2e^2/h$, with additional plateaus appearing near e^2/h under certain conditions. In single-walled nanotubes, multiple steps in dc current were reported in devices with highly resistive metal contacts [5, 6] and were attributed to populating higher 1D subbands.

9.2.2 Materials and methods

The nanotubes used in this study were grown by chemical vapor deposition (CVD) from Fe catalyst on doped Si wafers (which serve as back gates) with 1 μm thermal SiO_2 and contacted with $\sim$ 15 nm of Pd [81]. All measured devices had nanotube diameters in the range $\sim$ 1.5-5 nm (actual diameters noted in figure captions). While we cannot exclude the possibility that our nanotubes are small ropes or double walled tubes, all devices for this study can be fully depleted with the back gate. Therefore, it is likely that only a single semiconducting tube is participating in transport. In addition, using TEM analysis of nanotubes grown under similar conditions we were able to distinguish between large ropes and single tubes. Further, we were unable to observe any internal structure in single tubes with diameters less than $\sim$ 4 nm.

In some cases, the nanotubes were pushed with the tip of an atomic force microscope (AFM) to form a bend [131, 27, 20]. Three device configurations were investigated: bent tubes with side gates (Fig. 9.3b, inset), as well as unbent and bent tubes with local electrostatic top-gates (Fig. 9.5a, inset). It has previously been shown that bends create gatedepletable regions [131, 20], and that local gates affect only proximal sections of the tube [111]. The top-gated devices were made by depositing CVD-grown SiO_2 on the Pd-contacted nanotubes and patterning Cr/Au gates using electron-beam lithography [111, 166]. Two-terminal differential conductance, $G = dI/dV$, was measured as a function of source-drain bias, V_{SD}, by applying dc + ac voltage, $V = V_{SD} + V_{ac}$ (with $V_{ac} \sim$ 50-180 μV), and separately measuring dc and ac currents. Fourteen devices in these configurations showed qualitatively similar behavior.

9.2.3 Conductance plateaus in a side-gated device

Figure 1(a) shows characteristic plateau features in dI/dV for an intentionally bent tube (device shown in Fig. 9.3b) as a function of source-drain voltage, V_{SD}, with the voltage on a local side gate near the bend, V_{SG}, held fixed for each trace. Plateaus appear as bunched traces where the conductance changes little as V_{SG} is changed. These plateaus are also apparent in slices taken at fixed V_{SD} (colored vertical lines in Fig. 9.3a) as a function of V_{SG}, as shown in Fig. 9.3b. In this device, high-bias dI/dV saturates at $\sim 3.3\ e^2/h$, somewhat below the ideal value of 4e2=h, presumably due to backscattering at the contacts or within the tube. To account for this, a series resistance, R_S, is subtracted to bring the high-field saturation to $\sim 4e^2/h$. Several plateaus are visible, at both low and high bias ($V_{SD} \sim 30$ mV), spaced by roughly e^2/h. Plateaus around zero bias show considerable overshoot, while those at high bias are typically much flatter. Smooth evolution between these two sets of plateaus with changing V_{SD} is also evident, and revealed more clearly in Fig. 9.4. Conductance shows a dip around zero bias that deepens as temperature is lowered. Further, near $V_{SD} = 0$ at temperatures below ~ 15 K, single-electron charging is evident when the conductance is below the first plateau (Fig. 9.3c), while in the high conductance region, a Fabry- Perot-like interference pattern is observed (Fig. 9.3d) [102]. Irregularity in the interference pattern may be due to scattering from intrinsic defects in the nanotube, but the persistence of Fabry-Perot interference implies that this scattering does not significantly affect ballistic transport in the device. The Fabry-Perot structure and the zero bias dip may affect the positions of the plateaus, especially near $V_{SD} = 0$.

9.2.4 Transconductance

The transconductance, dG/dV_{SG}, for the same device (inset Fig. 9.3(b)) is shown in Fig. 9.4a. Transconductance highlights transitions between plateaus as bright regions, with dark regions representing the plateaus. Figure 9.4(a) shows that as $|V_{SD}|$

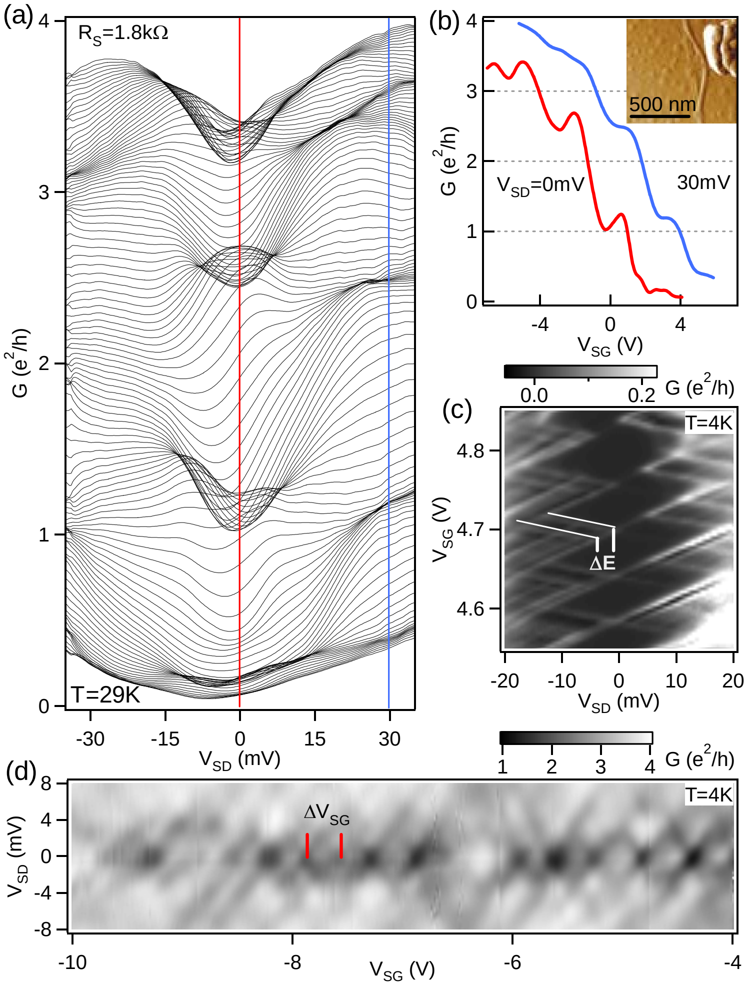

Figure 9.3: (a) Differential conductance $G = dI/dV$ as a function of source-drain bias, V_{SD}, and side gate voltage, V_{SG}, for a bent nanotube device, diameter $d \sim 3.5$ nm, at temperature $T = 29$ K. Series resistance R_S is indicated. Traces are taken at fixed V_{SG}; bunched traces correspond to conductance plateaus. (b) Slices from (a) at fixed V_{SD}. The high-bias trace is offset by 2 V in V_{SG} for clarity. Inset: AFM image of the device, showing a tube pushed toward the side gate (top right). Total device length is ~ 1.5 μm. (c) G measured at 4 K for the same device with V_{SG} set below the first plateau where Coulomb blockade diamonds are evident. Typical excited state level spacings, ΔE, are 2-3 meV, corresponding to a device length $L \sim$ 500-700 nm. (d) G in the high conductance region ($G > e^2/h$), with Fabry- Perot interference period $\Delta V_{SG} \sim 0.3$ V. For this panel, series resistance $R_S = 1.2$ kΩ.

is increased, each transition splits into two which at larger bias recross, restoring the original number of plateaus. (It is near this recrossing value of bias, $V_{SD} \sim 30$ mV, that the high-bias cut in Fig. 9.3b is taken.) The resulting pattern of transitions can be interpreted in the context of transport through quantized modes: if one assumes that each transition corresponds to the entering of a 1D mode into the transport window, then the diamond pattern in dG/dV_{SG} follows the evolution of mode energies with V_{SD} and V_{SG}. This is the standard noninteracting picture of nonlinear "half plateaus" in quantum point contacts [60, 129].

Experimental dG/dV_{SG} (Fig. 9.4(a)) can be compared to various schemes for the evolution of 1D modes. In the simplest picture of four conduction modes with spin and band degeneracy [115], one expects a single transition from $G = 0$ to $G = 4e^2/h$ around zero bias as V_{SG} is increased, and a single half plateau with $G = 2e^2/h$ at high bias (Fig. 9.4b). With one degeneracy lifted (e.g., band degeneracy lifted by strain), the simple picture gives features as in Fig. 9.4c, with plateaus and half plateaus spaced by $2e^2/h$. With all degeneracies lifted, this picture gives four plateaus and four transitions each spaced by e^2/h, and half plateaus at 1/2, 3/2, 5/2, and 7/2 times e^2/h (Fig. 9.4d). Surprisingly, the experimental data most resemble the schematic in Fig. 9.4d.

9.2.5 Energy scales

Within an interpretation of separate 1D modes, positions of the half plateaus from Fig. 9.4a give a value for the 1D mode energy spacing of $\Delta_{1D} \sim$ meV between the first and the second plateau, with a spacing in $V_{SG} \sim 1.8$ V. Together, these give

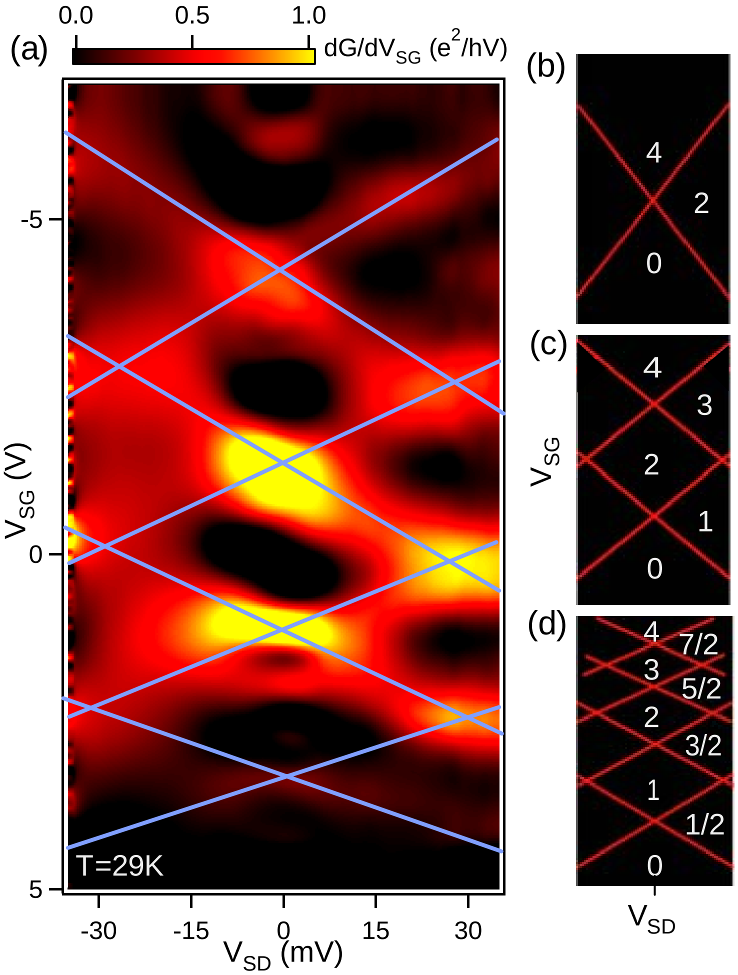

Figure 9.4: (a) Transconductance, dG/dV_{SG} as a function of V_{SD} and V_{SG} for data in Fig. 9.3(a). Dark regions correspond to plateaus, bright regions to transitions between plateaus. Blue lines are guides indicating the evolution of conductance modes with V_{SD} and V_{SG}. (b)(d) Models for transconductance evolution with gate voltage for a four-mode 1D conductor for the case of (b) fourfold degeneracy, (c) two-fold degeneracy, and (d) fully broken degeneracy. Numbers denote expected conductance values for plateaus in units of e^2/h (see text).

a coupling efficiency $\alpha \equiv \delta E / e\delta V_{SG} \sim 0.03$, which describes the shift of the Fermi level in the nanotube with V_{SG}. We distinguish between this coupling constant and the familiar lever arm (ratio of gate capacitance to total capacitance), extracted from Coulomb blockade diamonds. The quantity α characterizes a change in Fermi energy induced by a gate, in the present case dominated by a change in density.

The coefficient $\alpha = C_L/(e^2 \partial n/\partial \mu)$, where $C_L^{-1} = \left(C_L^G\right)^{-1} + (e^2 \partial n/\partial \mu)^{-1}$, contains both a geometrical capacitance per unit length, C_{GL} , and a term reflecting the kinetic energy (per unit length) required to increase the depth of the Fermi sea (n is the linear density and μ is the chemical potential). Since $\alpha \ll 1$ (kinetic capacitance dominates geometric), we may approximate $\alpha \sim C_L^G/(e^2 \partial n/\partial \mu)$. The kinetic component can be calculated from a linear dispersion relation, $\delta E = \hbar v_F \delta k$ and $\delta k = \pi \delta n/M$ (where M is the number of modes), giving $e^2 \partial n/\partial \mu = e^2/\pi \hbar v_F \sim 100$ pF/m per mode, where $v_F \sim 8 \times 10^5$ m/s is the typical Fermi velocity. The measured value $\alpha \sim 0.03$, extracted when only one mode is present, can then be used to calculate $C_L^G \sim 3$ pF/m.

The estimate of C_L^G above has assumed fully lifted degeneracies. This interpretation is supported by a comparison of the length of the mechanical bend (~ 500 nm) with the effective device length L associated with both Coulomb blockade and Fabry-Perot oscillations, determined using C_L^G . The period of Coulomb blockade oscillations, $\Delta V_{SG} = e(LC_L^G)^{-1} \sim 0.05$ V, which corresponds to the addition of one electron to a length L, gives $L \sim 1$ μm. The period in V_{SG} of the Fabry-Perot pattern corresponds to a change in wave vector by $\delta k_F = \pi/L$, hence a change in carrier density by $\delta n = 4\delta k_F/\pi$, taking all modes to be occupied near the highest plateau, where Fabry-Perot is measured. Relating the Fabry-Perot period $\Delta V_{SG} = 0.3$ V to density, $e\delta n = C_L^G \Delta V_{SG}$, gives an independent estimate of effective device length, $L = 4e(\Delta V_{SG} C_L^G)^{-1} \sim 700$ nm, using C_L^G from above.

We note that interpreting the measured half-plateau positions in terms of 1D subbands would require a nanotube diameter of $\sim$ 15 nm, inconsistent with AFM measurements for all devices. If the band structure of the nanotube were modified substantially by the presence of a mechanical defect and a nonuniform gate, the 1D subband spacing could be reduced to the values we observe [122]. However, the appearance of plateaus spaced by e^2/h is not to our mind explained by the influence of defects, nor by other structures such as multiple nanotube shells.

9.2.6 Device geometry dependence of plateau spacing

In all measured devices, dI/dV was everywhere less than $4e^2/h$. Subtracting R_S to bring the large-bias conductance to $4e^2/h$ typically yielded plateaus and half plateaus spaced by $\sim e^2/h$. In no case could we subtract an appropriate R_S to give plateaus separated by $2e^2/h$ or $4e^2/h$. Series resistance is presumably dominated by contact resistance at the Pd-nanotube interface. However, back gate-voltage-dependent scattering within the tube away from the gated region may also contribute.

Figure 9.5 demonstrates the effect of the gates in producing spatially localized depletion regions. Conductance of an unbent tube with two top gates shows plateau structure as a function of either gate. The two gates evidently act independently, each depleting different regions of the tube, leading to the square pattern seen in the inset of Fig. 9.5a. Two gates influencing the same region of the tube would produce a diagonal pattern instead.

Three of the measured devices showed a nonconductive region as a function of gate voltage with high conductance regions on either side, presumably reflecting an energy gap in a semiconducting nanotube [109]. Data for one such device, an intentionally bent tube without local gates, are shown in Fig. 9.5(b). Both the holelike regime (at negative gate voltage), and the electronlike regime (at positive gate voltage) show e^2/h conductance plateaus as a function of gate voltage. Figure 9.5c shows plateau structure with spacings of $\sim e^2/h$ in another bent-tube device as a function of top gate voltage over the bend and V_{SD}.

9.2.7 Effect of temperature and magnetic field

Figure 9.6 shows the low-bias conductance plateaus of the side-gated device (Fig. 9.3b, inset) as a function of temperature and magnetic field. No series resistance has been subtracted from these data. The plateau near e^2/h, which shows considerable overshoot at low temperature, rises to a value close to $1.5e^2/h$ with increasing temperature, while the subsequent plateaus are smoothed with increasing temperature but do not rise significantly. Plateaus measured for this device at high bias show little change with increasing temperature. Magnetic field applied perpendicular to the tube axis has little effect on plateau structure (Fig. 9.6b). Here, the Zeeman splitting at $B =$ 8 T, $g\mu_B B \sim 0.9$ meV, is greater than thermal energy ($k_B T \sim 0.15$ meV) but less than the voltage bias ($eV_{SD} = 2$ meV). Comparable ratios of magnetic field to bias energies induce significant change in $G(V_G)$ curves in GaAs quantum point contacts with spin degenerate levels.

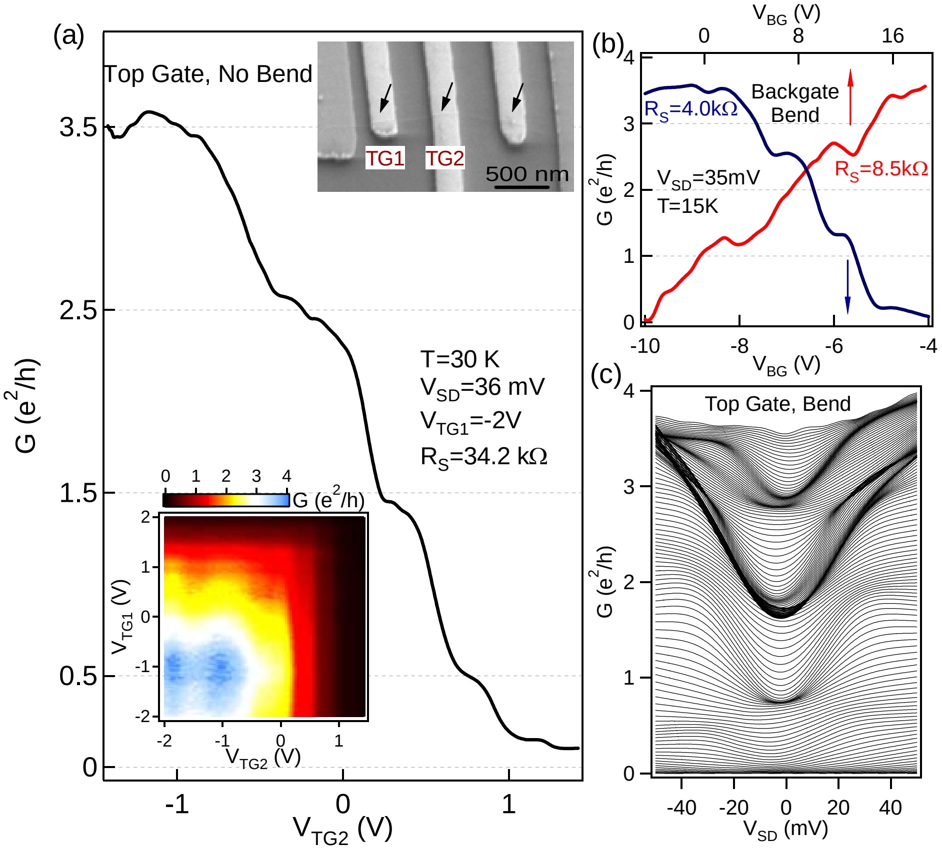

Figure 9.5: (a) Differential conductance G as a function of gate voltage for an unbent nanotube, $d \sim 1.5$ nm, with top gates, showing plateaus spaced by $\sim e^2/h$. Upper inset: SEM of measured device. The nanotube (arrows) is visible under the SiO_2 and top gates. Lower inset: G as a function of two top gates, with $V_{SD} = 36$ mV. (b) $G(V_{BG})$ at $V_{SD} = 35$ mV for another device, with $d \sim 3.2$ nm. Conductance plateaus appear for both hole (blue trace, bottom axis) and electron (red trace, top axis) transport. Different series resistances have been subtracted from the traces as noted on the figure. (c) G as a function of V_{SD} and top gate voltage at $T = 50$ K for a bent-tube device, $d \sim 4.5$ nm, with a top gate. $R_S = 11.8$ kΩ.

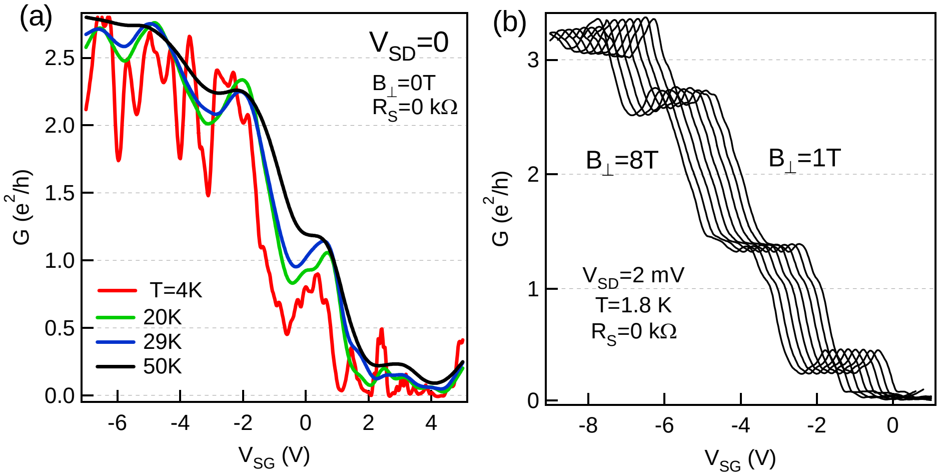

Figure 9.6: (a) Temperature dependence of conductance plateaus around $V_{SD} = 0$ for the device in Fig. 9.3(b) (inset). (b) Evolution of the low-bias conductance plateaus for the same device (different cooldown) in a magnetic field perpendicular to the sample plane with $V_{BG} = 0.68$ V. Curves are offset in V_{SG} for clarity. No series resistance is subtracted in (a) or (b).

9.2.8 Conclusions and acknowledgements

Possibly relevant to our results is the appearance of a zero-magnetic-field conductance plateau near e^2/h [135], or more commonly closer to $0.7(2e^2/h)$ [148, 39, 42], in gate-defined semiconductor quantum point contacts and wires. A theoretical model of this so-called 0.7 structure in quantum point contacts involving the formation of an ordered electronic state in 1D [113] may be relevant in nanotubes as well. We note that previous studies of Pd nanowires have observed conductance plateaus at $\sim e^2/h$, which the authors suggested may indicate ferromagnetism or near-ferromagnetism in Pd nanostructures [136] (though $\sim e^2/h$ plateaus were also seen in similar Ti structures). The plateau structure reported here is most evident in Pd-contacted nanotubes; however, we believe this is primarily due to the highly transparent contacts obtained with Pd rather than an effect of nearferromagnetism in the leads, as magnetic field sweeps at both high field and around zero field showed no hysteresis or change in plateau structure. Finally, it is possible that the observed quantization of conductance in units of $\sim e^2/h$ may be due to Luttinger liquid renormalization of 1D subbands of the nanotube, as writing $G = g(e^2/h)M$ with $M = 4$ the number of modes per subband and $g \sim 0.28$ the Luttinger parameter produces quantization near e^2/h.

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Appendix A

A low-temperature atomic layer deposition liftoff method for micro- and nanoelectronic applications

One technical development which came early in my graduate career was the formulation of a method to pattern of high quality dielectric layers without etching (this being derived at least partially from my reservations about using HF as an integral component of device processing). In this Appendix I will present a technique developed in our lab for the lift-off patterning of dielectric films deposited by atomic layer deposition.

A.1 Introduction

A variety of applications require thin film oxides as gate dielectrics, simple insulators, or protective coatings. The push for dielectric layers exhibiting high conformality, uniform stoichiometry and thickness, large breakdown fields, and high dielectric constants has motivated a search for alternatives to SiO_2 and associated deposition techniques [165, 66]. Chemical vapor deposition (CVD) provides highly uniform films on the wafer scale but requires high growth temperatures, which can damage underlying layers as well as polymer resists [132]. Sputtering and evaporation can be performed at lower temperatures, but often produce dielectric films that suffer from pinholes, poor conformality, and poor adhesion to the substrate [132].

An emerging deposition technique that offers relatively precise control of composition, conformality over high-aspect-ratio structures, and thickness control is atomic layer deposition (ALD) [99]. ALD is a self-limiting deposition process where separate precursor gases for a target material are sequentially and cyclically dosed into a vacuum chamber under computer control. Substantial work has been invested to develop ALD processes that yield high quality films and use precursor gases that do not chemically damage preexisting device structures [71].

Previously, a significant shortcoming of ALD was that, like CVD, patterning of dielectrics required a subtractive process, in which whole layers were deposited, and patterning was done by etching. This limitation arose from the need to use deposition temperatures exceeding 300 C, which destroyed resist layers or caused them to outgas and disrupt film growth. In precise applications, etch steps are often unacceptable as they can damage other device structures. Moreover, it is difficult to pattern fine features by etching; first, because any subtractive process requires leaving a patch of resist on the 3 substrate the same size as the desired feature, and second, because low energy dielectric etches (which do not damage the device) are generally isotropic, causing feature shape change and undercutting [132]. In contrast, liftoff patterning allows one to cut a "slit" in a resist layer and deposit material only where needed. It is therefore desirable to develop liftoff processes for dielectrics similar to those used for metallization. High quality dielectric films patterned by liftoff would be of great value not only in the semiconductor industry, but also in optical applications [160, 151], as catalysts [121, 7], and as protective coatings [77, 162]. We note that although polymer resists have been used previously in crudely patterning ALD films for profilometry measurements, actual liftoff lithographic patterning has not been reported to date [50].

In this Appendix we demonstrate a process that allows ALD-grown dielectric films to be patterned using liftoff. Examples described in detail are the highκ materials aluminum oxide (Al_2O_3) and hafnium oxide (HfO_2). The ALD process employed operates at low temperature and uses non-corrosive precursor gases. The patterned films are uniform in thickness with deviations $\sim$ 1 nm, and are conformal to underlying device structures. ALD liftoff is demonstrated for both photolithography and electron-beam lithography, yielding films with patterned features below 100 nm. We have also measured the dielectric constants and breakdown fields of comparably grown unpatterned films of Al_2O_3, HfO_2 and ZrO_2, finding $\kappa \sim$ 8.2–9 for Al_2O_3, $\kappa \sim$ 16.3–18.5 for HfO_2, and $\kappa \sim$ 20–29 for ZrO_2, at various film thicknesses and measurement temperatures. All films measured exhibit breakdown fields between 5.6 and

9.5 MV/cm, varying with material, film thickness and measurement temperature (see Table A.1).

A.2 Methods

A.2.1 Lithographic patterning

The photolithographic ALD process consisted of the following steps. First, cmscale pieces of a polished Si wafer with 1m of thermally grown oxide were cleaved, cleaned (5 minutes in each of tricholoroethlyene, acetone, methanol) and baked for 5 minutes at 160 C to drive off solvent residues. Next, Shipley 1813 or 1818 photoresist was spun onto the samples, after which they were baked for 2 minutes at 120 C and exposed through a photomask with large features (> 10 μm). Patterns were developed using tetramethyl ammonium hydroxide and cleaned for 30 s in 100 W oxygen plasma at 700 mtorr. Thin films were then grown on these samples via ALD, as described below. The electron-beam ALD process, used for fabricating fine features, began with similar Si samples, cleaved and cleaned using the same three-solvent rinse followed by a 2 minute bake at 180 C. A bilayer of 200 k PMMA and 950 k PMMA was spun onto a sample and baked for 15 min at 180 C for each layer, yielding a total PMMA thickness ~ 350 nm. Fine-line patterns were written and developed in a solution of isopropanol (75%) methyl isobutyl ketone (24%), and methyl ethyl ketone (1%).

A.2.2 Film deposition

The ALD procedure used for both the photolithographic and electron-beam liftoff processes employed highly reactive metal amide precursors (tetrakis(dimethylamido)hafnium (IV) and H_2O for HfO_2; tetrakis(dimethylamido)zirconium (IV) and H_2O for ZrO_2 [71, 63, 62, 61], and trimethylaluminum and H_2O for Al_2O_3 [128, 112, 133]). Samples were placed in a stainless steel tube furnace and heated to 100-150 C. The cycle of precursors was then started, with nitrogen purges between each step. In order to achieve low-temperature deposition with uniform thickness, the nitrogen purge time needed to be lengthened (from $\sim$ 5 s, used for the 300 C process, to $\sim$ 120 s) to prevent physisorption and to remove unreacted gas-phase precursors. Film thicknesses ranged from 2.5 to 100 nm.

Despite the reduced temperature and lengthened total deposition time, the films appear similar in composition to those grown at higher temperatures, although some important differences exist. First, while surface roughness of these films is typically 5% of total film thickness for high temperature deposition ($>$ 200 C) it is less than 1% total film thickness for deposition temperatures below 150 C, except where limited by substrate roughness [72]. Second, X-ray diffraction data indicate that 100 nm thick films of unpatterned HfO_2 grown at or below 100 C are completely amorphous while those grown at higher temperatures show some crystallinity (<10% for growth temperature up to 200 C) [72]. Low-temperature grown ZrO_2 films characterized in the same manner show an increase in crystallinity from 10% to 60% as the deposition temperature increases from 100 to 150 C [72]. It is worth noting that amorphous dielectric films are desirable for applications as gate dielectrics due to their smoothness and high breakdown fields compared to polycrystalline films [12, 97].

A.2.3 Liftoff

Following the growth step, the liftoff procedure was carried out by immersing samples in acetone for times ranging from 10 m to 2 h. To allow the acetone to penetrate the conformal dielectric layer and attack the resist below, it was necessary to manually scratch the surface of the film. While still immersed in acetone, ~ 1 s pulses from an ultrasonic bath were used to dislodge remaining sections of resist.

A.3 Characterization

A.3.1 AFM

Atomic force microscope images in Fig. A.1 show that the resulting patterned films have surface roughness comparable to that of the SiO_2 substrate (~ 1 nm), and sharp step edges. Deviation of the edge from a straight line is limited by the photolithography and not film deposition or liftoff. This was verified by examining metal lines deposited in similar patterns, as shown in Fig. 4. Micrographs of patterned ALD films on SiO_2 (Figs. A.1(a) and A.2(a)) show edge roughness ~ 10 nm for electron-beam patterning and ~ 100 nm edge roughness for photolithographic patterning (Figs. A.1(b) and A.2(b)).

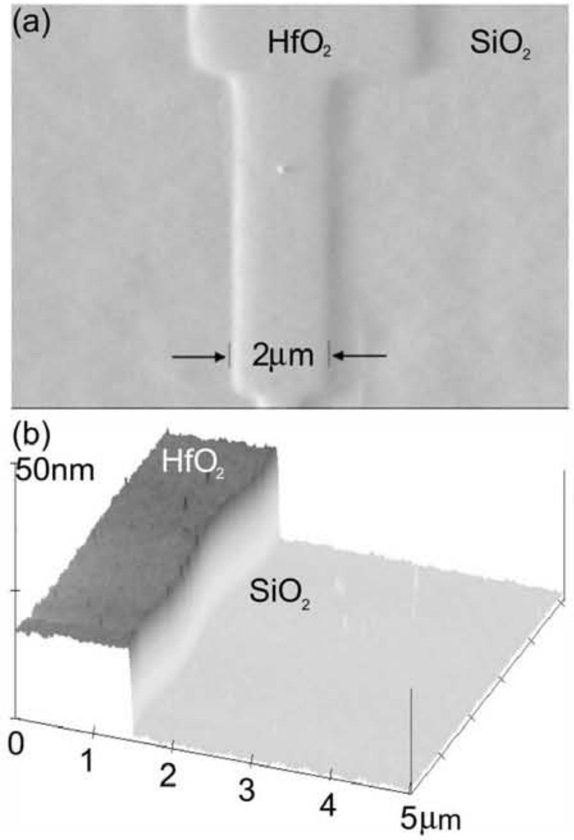

Figure A.1: Atomic force micrographs of patterned ALD oxides on a Si/SiO$_2$ substrate. (a) A 15 nm thick narrow line of oxide patterned via electron-beam lithography necks down from 5 μm to 1 μm (top to bottom). Note the vertical edge profile on both sides of the line and edge smoothness. (b) AFM surface plot of a $\sim$ 22 nm thick mesa of ALD oxide patterned by photolithography shows a well defined and highly vertical step. The waviness seen in the edge is limited by the photolithography.

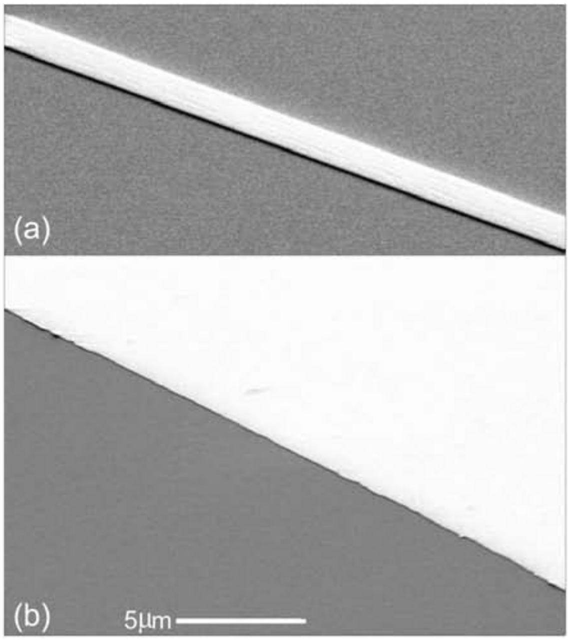

Figure A.2: Scanning electron micrograph showing the smooth edge profiles of ALD patterned via (a) electron-beam lithography, (b) photolithography. Surface roughness was $\sim$ 1 nm as analyzed by AFM (Shadows result from high-angle imaging).

A.3.2 SEM

Figure A.3 shows an SEM image of a device geometry featuring lines of dielectric patterned via electron-beam lithography, with smallest dimensions below 100 nm. We have also fabricated complicated multilayer device geometries in which metallic layers are partially coated with patterned ALD films, followed by patterned metallic overlayers. SEM analysis shows (Fig. A.4) that patterned ALD films running over metallic lines are highly conformal around the metal line edge and at the metal-substrate interface.

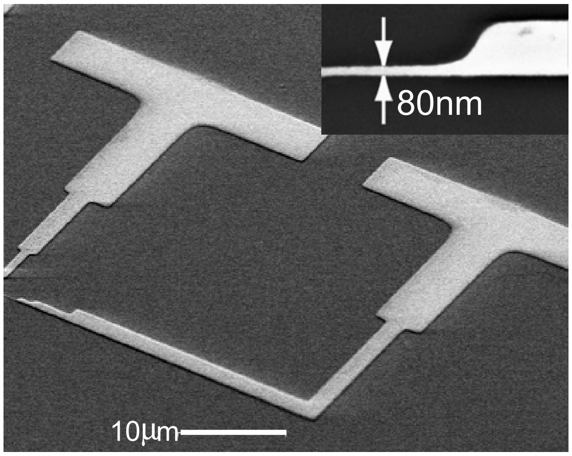

Figure A.3: SEM image of 15 nm thick HfO_2 on Si/SiO_2, patterned by electron beam lithography. Device critical dimensions ∼ 80 nm as measured using the SEM. Inset: region of the device showing smallest features.

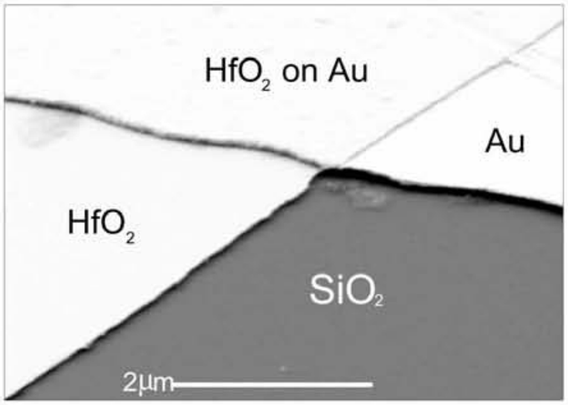

Figure A.4: Multilayer structure (30 nm ALD oxide and 70 nm Ti/Au, both patterned using photolithographic liftoff) showing high conformality of the ALD around the edge of the Ti/Au.

A.3.3 Electrical

The dielectric constants and breakdown voltages of unpatterned dielectic films grown by low-temperature ALD as described above were measured as follows. Films of Al_2O_3, HfO_2 and ZrO_2 were grown on Si-SiO_2 substrates with 20 nm Ti + 50 nm Pt electrodes deposited by electron-beam evaporation. ALD films were deposited at 150 C and showed good adhesion to the Pt underlayer. Subsequently 50 nm Pt was evaporated through a shadow mask to form a top electrode of dimension ~ 200 μm $\times$ 200 μm. These tri-layer structures formed parallel-plate capacitors, which were characterized in a vacuum probe station at 20 K and room temperature. A 1 kΩ resistor was placed in series with these test devices, and digital lock-ins were used to measure the voltage drops across both the resistor and the test device. The circuit was voltage biased using a function generator with an excitation of ~ 100 mV at 1 kHz. Voltages across the resistor (V_R) and test device (V_C) were used to measure the capacitance of the test device, $C = V_R(2\pi f R V_C)^{-1}$ and hence the dielectric constant of the film, $\kappa = Cd/A\varepsilon_0$ (A is the device area; d is the film thickness). Dielectric constants $\kappa \sim$ 20–29 are found for ZrO_2, $\kappa \sim$ 16–19 for HfO_2, and $\kappa \sim$ 8–9 for Al_2O_3 (see Table A.1). Breakdown fields $E_{BD} = V_{BD}/d$ were found by applying an increasing dc bias until the onset of a large leakage current was observed at V_{BD}. Values obtained are in the range $E_{BD} \sim$ 6–9 MV/cm for all three materials, approaching the breakdown fields for high-quality SiO_2 films. Resulting values for dielectric constants, breakdown fields, and calculated charge densities presented in Table A.1 for varying thicknesses and measurement temperatures of the materials. It is interesting to note that the values we obtain for breakdown fields in these devices are

Material	d (nm)	T_M	E_{BD} (MV/cm)	κ	Q_{BD} (μC/cm^2)
Al_2O_3	10	RT	8	9	6.4
Al_2O_3	2.5	RT	8.3	8.8	6.5
Al_2O_3	25	RT	8.2	8.2	6.0
Al_2O_3	50	RT	7.6	8.9	6.0
ZrO_2	25	RT	5.6	20	9.9
ZrO_2	100	RT	6	29	15.5
ZrO_2	50	20K	8.2	29	21
ZrO_2	100	20K	9.5	26	22
HfO_2	10	RT	6.5	17	9.7
HfO_2	25	RT	7.4	18.5	12
HfO_2	25	20K	8.4	16.3	12.1

Table A.1: Properties of several high-κ materials grown using the same low-temperature ALD process as used for liftoff, measured at 20 K and room temperature (T_M): breakdown field, $E_{BD} = V_{BD}/d$ (V_{BD} is breakdown voltage, d is film thickness), dielectric constant κ (see text), and charge density at breakdown, $Q_{BD} = CV_{BD}$.

two to three times higher than those previously reported in the literature for HfO_2 and ZrO_2 [116, 108, 89]. We believe the difference is due to the low-temperature growth process, which produces amorphous films.

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Appendix B

Transport measurements on undergated nanotube devices

B.1 Transport measurements

Transport measurements were made on the devices described in section 3.2.1 at 4K using a dc voltage bias, V = 10 mV, and measuring dc current, I. Data is presented for a single device (Fig. B.1); similar behavior was observed for other devices. Conductance, $G = I/V$, was measured as a function of voltages applied to various finger gates and the backgate. Sweeping the backgate with the finger gate voltages held fixed at 0V produces rapidly varying, reproducible fluctuations in G as a function of backgate voltage, V_B (Fig. B.1b). The $G(V_B)$ data show that the SWNT is likely metallic, as there is no significant trend in conductance peak height as we move from positive to negative values of V_B. The rapid fluctuations are presumably due to Coulomb blockade resulting from quantum dots defined by scattering centers along the tube, although it is unclear if the scattering centers are innate or caused by the presence of the underlying finger gates. The lack of symmetry within the Coulomb fluctuations is consistent with the presence of multiple quantum dots in series. The backgate seems to couple to all of these dots simultaneously and is capable of rearranging charges between the dots [145].

Sweeping the voltage on individual finger gates produces qualitatively different behavior in the conductance. In this case, we observe smooth changes in G as a function of all of the finger gate voltages (Fig. B.1a). One of the gates ($F5$) exhibits a broad resonance feature. Setting a single finger gate to a nonzero voltage, V_F, with the other finger gates held at zero again yields rapid fluctuations in $G(V_B)$, but with different overall amplitude, consistent with the $G(V_F)$ from Fig. B.1a acting as an overall smooth envelope of $G(V_B)$. Examples of $G(V_B)$ for two settings of V_F on $F4$ are shown in Fig. B.1b; similar behavior was observed with other finger gates.

The qualitative difference between the effects of the backgate and finger gates suggests that the finger gates act to locally tune the transparency of the aforementioned scattering centers. This picture is supported particularly by the nonmonotonic (resonant-like) behavior of $G(V_{F5})$. Local scatterers have previously been linked to the formation of intratube quantum dots [145, 35, 115] and have been observed by scanned gate measurements [56, 26, 145] and electrical-force microscopy [168]. Additonally, gate $F1$, located under the SWNT-metal contact could be tuning the transparency of the tunnel barrier formed at the metal-nanotube interface. If the finger gates were instead having a global effect and coupling to the entire tube device, one would expect Coulomb-blockade phenomena very similar to those caused by sweeping the backgate, though perhaps on a different overall voltage scale.

Figure B.1c shows device conductance as a function of both backgate and finger gate voltages for the case where all finger gates are swept together. Fluctuations in $G(V_B)$ with $V_F = 0$ V previously described appear again but now evolve continuously into oscillations in $G(V_F)$ with $V_B = 0$ V, demonstrating the approximately additive behavior between V_B and V_F when all finger gates are swept. Evidently, when all finger gates are swept, they together do produce an effective global gating effect much like the backgate, albeit on a reduced voltage scale (as expected given the distances and dielectric constants). Thus although the effect of the individual finger gates is spatially localized along the nanotube, the area of influence appears to be larger than that defined by the physical dimensions of the finger gates. When the gates are utilized simultaneously, the collective area of influence encompasses the entire device.

As a direct comparison, Fig. B.1d shows corresponding plots when sweeping just one of the finger gate with the other finger gates held at 0 V. In this case, there is no additive effect evident between finger gate and back gate, even over an expanded range of V_F. Horizontal slices of the 2D plot show roughly the same behavior in $G(V_F)$ as observed at $V_B = 0$ V in Fig. B.1a (ignoring switching noise) while vertical slices show that oscillations in $G(V_B)$ persist for all values of V_F.

B.2 Conclusions and acknowledgements

In summary, we have demonstrated a method for local gating using finger gates beneath a catalyst-grown single-wall nanotube. The fabrication process takes advantage of robust Mo finger gates and liftoff-patterned dielectric films deposited by low-

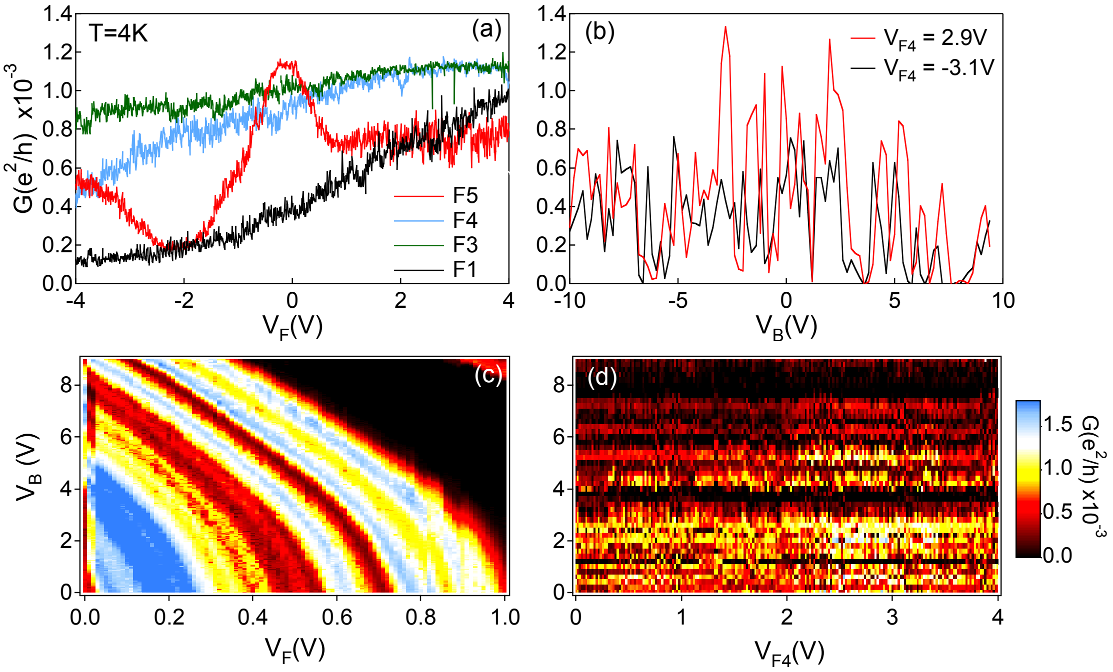

Figure B.1: Transport measurements taken from the device depicted in Fig. 3.1. All data taken at 4K. a) Conductance as a function of various finger gate voltages. Each trace represents the effect of a single finger gate swept from +4 V to -4 V while all others, including the backgate, are set to 0 V. Gate $F2$ showed significant leakage above $V_{F2} \sim 2V$ and so was not included in these plots. b) Charging effects observed by sweeping the Si backgate. Traces are displayed for two different voltages on finger gate $F4$, which changes the overall magnitude of the rapid fluctuations without changing the qualitative structure. c) Color plot of conductance as a function of backgate voltage (V_B) and common finger gate voltage (V_F) (i.e. all finger gates swept together) indicating an additive effect of V_B and V_F. Color scale shows conductance in units of e^2/h. d) Comparable color plot showing conductance as a function of V_B and a single finger gate at V_F with other finger gates set to V=0.

temperature atomic layer deposition. Future applications of the technique reported include fabricating multigate nanotube FETs or quantum dots with independent control.

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