LOW TEMPERATURE TRANSPORT IN QUANTUM DOT ARRAYS

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By

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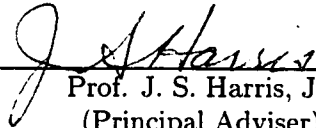**UMI**
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Prof. J. S. Harris, Jr.
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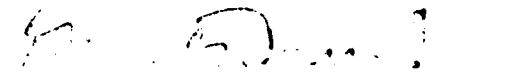
_____
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(Co-adviser)

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Doctor of Philosophy.

_____
Assist. Prof. C. M. Marcus

Approved for the University Committee on Graduate Studies:

_____

to my parents, sister and ...

The man bent over his guitar
A shearsman of sorts. The day was green.

They said, "You have a blue guitar,
You don't play things as they are."

The man replied, "Things as they are
Are changed upon the blue guitar."

Wallace Stevens

Acknowledgements

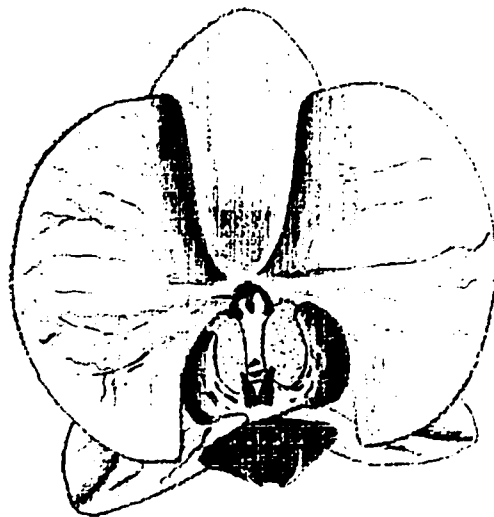# Abstract

In this dissertation, the results of the low temperature transport measurements in 200×200 quantum dot arrays will be presented and discussed [21]. The devices are made of $GaAs/AlGaAs$ two dimensional electron gas (2-DEG) structures, grown by Molecular Beam Epitaxy (MBE). The 2-DEG is processed using electron beam lithography and etching techniques to fabricate the arrays in which coupling between dots and electron density are controlled by a single gate. The devices measured within the scope of this thesis constitute the first controllable semiconducting quantum dot arrays in which possible collective effects and their relation to the strength of dot-to-dot interactions can be studied.

The current-voltage (I-V) characteristics of the arrays have two main features:

- At low temperatures, the current is zero below a threshold voltage, and above a threshold voltage increases obeying a power law with an exponent $\zeta \sim 1.5$. This is the first observation of a conduction threshold and metal-insulator transition in a semiconducting quantum dot array.

- There are discontinuous and hysteretic jumps in the current, or "switching events". Multiple switching events result in a hierarchy of hysteresis loops. This dissertation presents the first observation of such multi-stabilities in an array of semiconductor quantum dots.

These features in the I-V curves are very similar in appearance to those observed in a variety of other strongly interacting systems, including sliding charge density waves (CDW's) [35] and magnetically induced Wigner solid (MIWS) systems [4]. By

changing the gate voltage V_g, it is possible to move between the hysteretic and non-hysteretic regime. This also resembles the dynamics of the CDW's where switching and hysteresis are known to be highly temperature dependent [37, 95]. In a control dot fabricated on the same chip, a single hysteresis loop accompanied by a single switching event is also observed. This is different than the behavior of most top-gated quantum dots studied so far, an exception being the hysteresis observed by Wu et al. [94] in double barrier lateral structures.

Three kinds of devices will be considered in this dissertation.

- $1000\AA$ deep etched arrays. These are the devices (arrays and control devices) which showed conduction threshold, switching and hysteresis. They will be referred to as *Device 1, Device 2, Device 3, Device 4*. In Chapter 2, their fabrication will be described. In Chapters 3 and 4, the experimental data from these devices will be presented. The weak localization in these arrays as a function of the gate voltage will be briefly mentioned in Appendix C.

- $300\AA$ shallow etched arrays. These are the devices (arrays) which did not show switching and hysteresis. They will be referred to as *Shallow Devices*. The results of the gate current measurements in these devices will be discussed in Sec. 5.2.

- Three lead single dot. Coulomb Blockade in this split gate (See Sec. 1.2.1) device will be described in Sec. 5.2.2. These results represent the first measurement of Coulomb interactions in a three lead dot.

In Chapter 5, the possible mechanisms for hysteresis, such as charge exchange in the form of a leakage current to the gate, DX Centers and occupation of impurity states, and electron heating will be discussed. The experimental results will be compared to the characteristics of CDW and MIWS systems, in Sec. 5.5.

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Chapter 1

Introduction

1.1   Low Dimensional Quantum Structures

With the development of modern epitaxial growth techniques such as Molecular Beam
Epitaxy (MBE), it has become possible to grow structures with atomically smooth
interfaces and a very small number of impurities and defects. This facilitated the
design of structures in which carriers are confined in a plane perpendicular to the
growth direction (z), without experiencing significant scattering in the other two di-
rections, x and y. A particular example is the modulation doped $GaAs/AlGaAs$
two dimensional electron gas (2-DEG) structure in which the donors and the carriers
(electrons) are spatially separated from each other. In such a 2-DEG, the ionized im-
purity scattering is much less significant than in Si MOSFETs and $GaAs$ MESFETs
[77]. Together with the low density of imperfections due to optimized MBE growth
conditions[1], this results in an electron scattering time, $\tau = m\mu/e$, on the order of
$50ps$, and a mean free path, $l_e = v_F\tau$, as high as $10^4 nm$. Here μ, e and v_F denote the
electron mobility, charge and Fermi velocity, respectively. At low temperatures, the
phase coherence length, l_ϕ, can also become larger than $100nm$.

   As a result of the recent advances in electron beam lithography (e-beam lithogra-
phy), the modulation doped 2-DEG structure has become one of the most interesting

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[1]such as ultra high vacuum, typically 10^{-11} torr, high growth temperature ($640C$), and high
As/Ga flux ratio.
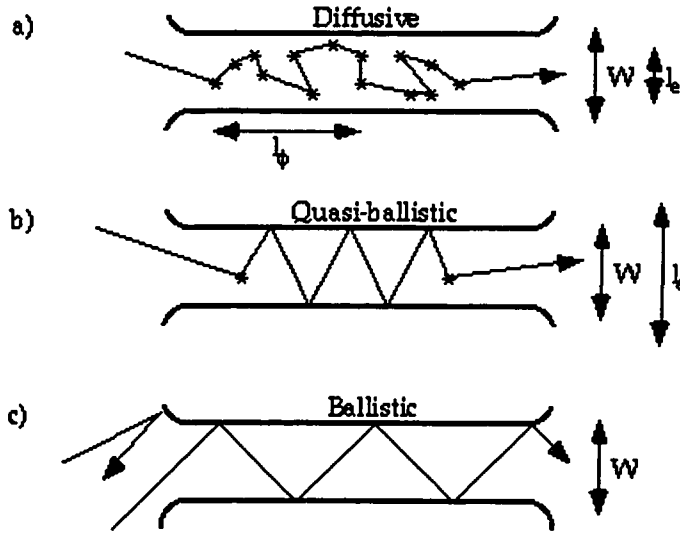
Figure 1.1: Typical Length Scales in a Semiconductor (From Ref. [10]).

two dimensional electron systems. By using e-beam lithography, it is possible to confine the electrons in one or two of the other directions, x and y, such that the device dimensions can become smaller than l_ϕ and/or l_e (Fig. 1.1).

For example, by depositing nanoscale split gates, quantum point contacts can be fabricated and at $4.2K$, conductance quantization can be observed [10]. Again, by depositing gates, "quantum dots" can be fabricated to study chaotic behavior of electrons [61]. The point contacts in a dot can be totally piched-off to form tunnel barriers. In this regime the dot is a 0-D device and at low enough temperatures, the blockade of tunneling due to Coulomb repulsion of electrons (Coulomb blockade [51, 42]) can be observed.

As these examples show, the developments in MBE and e-beam lithography, and their simultaneous use in the fabrication of low dimensional structures has resulted in the discovery of numerous important physical effects. In the next few sections, some

examples which are relevant to this dissertation will be described in detail.

1.2   0-D Structures:Quantum Dots

1.2.1   Tunneling and Coulomb Blockade

Blockade of electron tunneling due to Coulomb repulsion was first suggested in the 1950's and 1960's to interpret the results of transport experiments in granular metallic materials [33, 30]. Charge quantization was studied using a tunnel capacitor by Lambe in 1969 [53]. Nowadays, nanofabrication techniques like e-beam lithography and MBE make it possible to fabricate well controlled small tunnel junctions [20] and form metalic islands by cascading them. The Coulomb gap has been observed in the I-V curve of a single tunnel junction at low temperatures [79]. By cascading several *Al* tunnel junctions, frequency-locked turnstyle devices have been fabricated, and quantized current has been measured [28].

Detailed theoretical studies for Coulomb Blockade in metal tunnel junctions were made by Averin and Likharev [6, 8, 57, 7].

In semiconductors, the effect was first observed in *Si* quantum wires [80, 24]. Coulomb Blockade in these experiments resulted from the division of the quantum wire into segments separated by tunnel barriers formed due to impurities and disorder. Later, *GaAs/AlGaAs* 2-DEG quantum dots with split gates and a very small number of impurities were designed. This approach made it possible to form one of the conducting segments of the *Si* quantum wire artificially and controllably in single crystal *GaAs* [71, 43]. Later, many more experiments were carried out to study Coulomb blockade in *GaAs/AlGaAs* quantum dots [51, 49, 42, 5, 83]. Transport spectroscopy of the Coulomb island in the quantum hall regime was studied by McEuen et al. [66]. The quantized current in the presence of oscillating tunnel barriers was measured by Kouwenhoven et al. [50]. The same author and his co-workers also investigated photon assited tunneling [52].

Many theoretical studies were made simultaneously with the experiments. Meir and his co-workers studied the transport through quantum dots using a microscopic

model and a modified Landauer formula [69, 68]. The same author also calculated the low temperature regime using a similar formalism [70]. Beenakker used a semi-classical approach and obtained the same results for the conductance [9]. Korotkov studied the dot in the presence of a large coupling resistance [44, 45]. İmamoğlu and his co-workers calculated the I-V charactersitics in a micro p-N junction in the Coulomb blockade regime and predicted the generation of a regulated single-photon stream [40, 41].

Coulomb blockade oscillatons in the conductance of a quantum dot is the man-ifestation of single electron tunneling. The dot has to be isolated enough from the leads, such that the fluctuation of the charge Q inside the dot is negligible. This condition is equivalent to having tunnel junction resistances $R_T > R_Q$ where $R_Q = h/e^2 \simeq 25.8k\Omega$. Only an integer number of electrons can tunnel into the dot, and the charge inside the dot can only change by discrete amounts of e. If there are no offset charges, $Q = -Ne$ where N is the number of electrons which have tunneled into the dot. The potential between the dot and the leads can, however, be changed continuously by varying the voltage on one of the gates (Fig. 1.2).

Because of the Coulomb interaction, when an electron tunnels into the dot, the energy increases by an amount called the "Charging Energy", E_C. This increase can be characterized by assigning capacitance values between the dot and the gates, and between the dot and the semi-infinite leads. $E_C = e^2/C$, where C is the sum of all these capacitances [89]. When the gate voltage changes, a condition can be reached such that the energy is degenerate for two different electron charges Q and $Q - e$. This means that when this condition is satisfied, the tunneling event of an electron into the dot is favorable (Fig. 1.3). When the gate voltage is changed further, the device enters the Coulomb blockade regime again. There are conductance resonances whenever the energy is the same, for $Q - ne$ and $Q - ne - e$, where n denotes the number of extra electrons which are inside the dot due to a finite gate voltage. This means that the resonances are periodic.
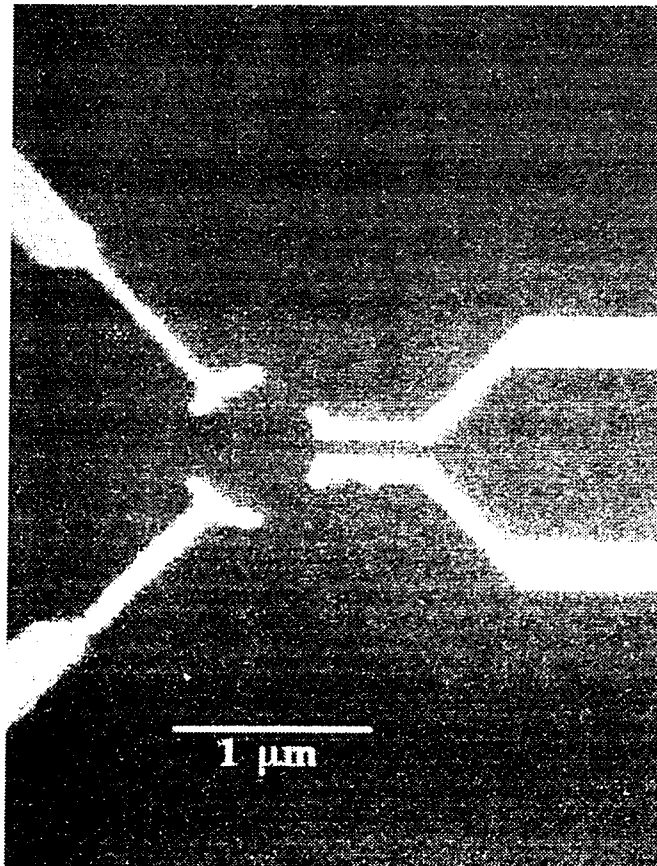
Figure 1.2: A split gate quantum dot.
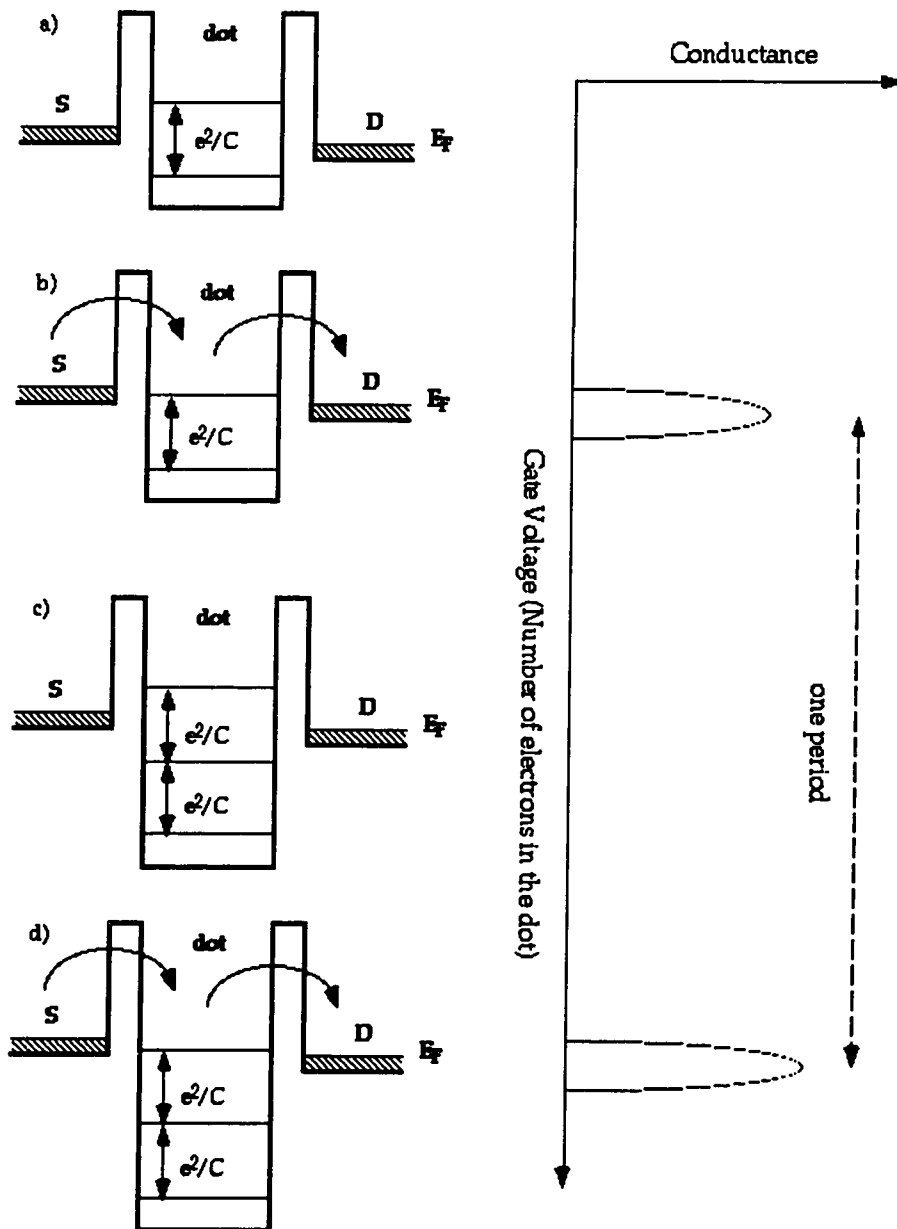
Figure 1.3: Coulomb blockade and Conductance Oscillations.

1.3 Quasi 1-D and 2-D Structures: Arrays

1.3.1 1-D Arrays

A natural question which arises after the study of single dots and metallic islands is the transport characteristics of a one or two dimensional array. This question becomes more interesting if there is significant interaction between the electrons in neighboring dots.

Most of the important experimental studies on one dimensional arrays of small tunnel junctions were done by Delsing et al. [19]. Using a simple circuit theory, it can be shown that, the potential, ϕ_i, at each node i of a one dimensional array is given by:

$$\phi_i = -\frac{e}{C_{eff}} \left(\frac{C}{C + C_0 + C_h} \right)^{|i-k|} \tag{1.1}$$

Here k is the index of the node at which there is an excess electron,

$$C_{eff} = \sqrt{(C_0^2 + 4CC_0)} \tag{1.2}$$

and

$$M^{-1} = \ln \left(\frac{C_{eff} + C_0}{C_{eff} - C_0} \right). \tag{1.3}$$

C_0 is the self capacitance of each electrode, C_h is the capacitance of a half infinite array, and C is the capacitance between electrodes. In these calculations, the capacitances between second and higher nearest neighboring islands are neglected. In most experimental situations, $C_0 \ll C$ so that the effective capacitance $C_{eff} \simeq \sqrt{4CC_0}$, and $M \simeq \sqrt{CC_0}$.

The potential falls off exponentially on both sides, as shown in Fig. 1.4. If an electron tunnels from electrode k to electrode $k \pm 1$, this potential distribution will move by one electrode preserving its shape. Therefore, it may be called a "soliton" [2]. An excess positive charge with its corresponding potential distribution is called "anti-soliton". The soliton extends over approximately $2M$ junctions and its energy E_S is

$$E_S = \frac{e^2}{2C_{eff}}. \tag{1.4}$$
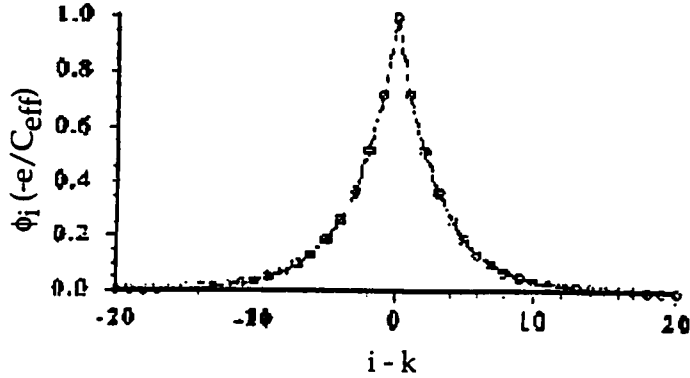
Figure 1.4: The potential distribution created by an excess electron on an electrode k inside an infinite 1-D array (From Ref. [18]).

The I-V charactersitics show an offset voltage, V_{off}, which is typical to the Coulomb blockade [18]. V_{off} depends linearly on the one dimensional array size. In the presence of microwave irradiation, there are additional current steps due to phase locking between the single electron tunneling oscillations and external microwave frequency [58].

Large one dimensional semiconductor quantum dot arrays in the Coulomb blockade regime have not yet been experimentally studied in detail. However, there has been some experimental [88] and theoretical [46] work on transport in double quantum dots.

1.3.2   2-D Arrays

2 Dimensional arrays of metallic Coulomb islands have been investigated both experimentally and theoretically. The early experiments on 2-D arrays were done by
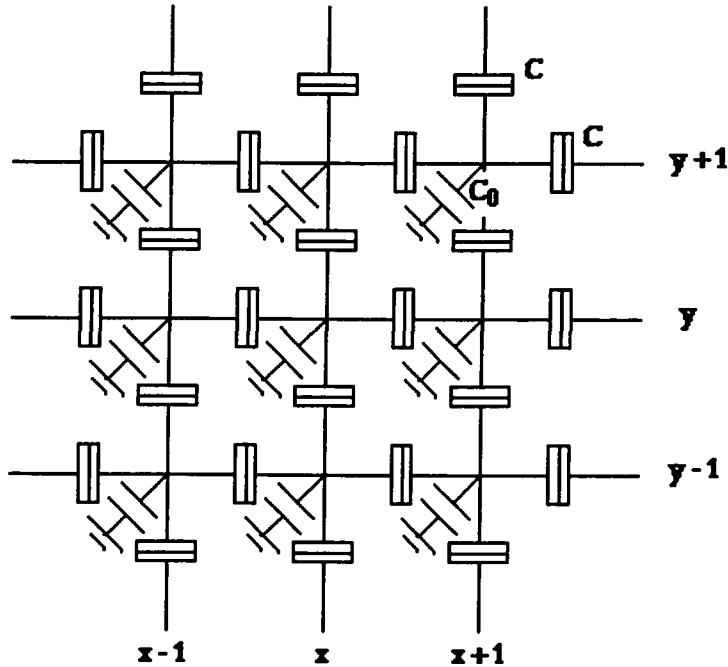
Figure 1.5: A schematic equivalent circuit for a 2-D array (From Ref. [73]).

Geerligs [27], Mooij [74] and their coworkers. For a two dimensional array, the charging energy can be expressed in terms of a capacitance matrix

$$H_{ch} = \frac{1}{2} \sum_{i,j} Q_i C_{ij}^{-1} Q_j,$$

where Q_i is the total charge on island i. It can only be an integer multiple of unit electronic charge, e. In a simple model, all the capacitances, except the capacitance between the nearest neighbors, C, and the self capacitance, C_0, can be neglected. A schematic diagram of the network is shown in Fig. 1.5.

As in one dimensional arrays, in most experiments $C_0 \ll C$. After writing a discrete Poisson equation

$$Q(x,y) = C_0\Phi(x,y)+$$
$$C\left[4\Phi(x,y) - \Phi(x-1,y) - \Phi(x+1,y) - \Phi(x,y-1) - \Phi(x,y+1)\right],$$

where $\Phi(x, y)$ is the electrostatic potential and taking the continuum limit

$$r = \sqrt{x^2 + y^2} \gg 1,$$

the equation

$$\nabla^2 \Phi(r) - \Lambda^{-2} \Phi(r) = 0$$

can be obtained [73]. In this equation, Λ is the screening length and is equal to $(C/C_0)^{1/2}$. The solution is $\Phi(r) = A K_0(r/\Lambda)$, where K_0 is the zero-order modified Bessel function and A is a constant. By Gauss' Law, A is found to be equal to $e/(2\pi C)$. For $r \ll \Lambda$ the Bessel function is equal to $-ln(r/\Lambda)$ and the potential is

$$\Phi(r) = -\frac{e}{2\pi C} \ln \frac{r}{\Lambda}, \qquad 1 \ll r \ll \Lambda.$$

This logarithmic interaction energy is that of a pair of opposite charges in a "Two-Dimensional Coulomb Gas". As the temperature is raised, more and more pairs are created with increasing separation. As soon as there is a pair with infinite separation, the conductance becomes finite. The corresponding temperature is T_{cn}, and near this transition temperature, the density of free carriers is given by

$$n_e(T) = K \exp \left[-\frac{b}{\sqrt{T/T_{cn} - 1}} \right]. \tag{1.5}$$

where K and b are constants. This is called the "Kosterlitz-Thouless-Berezinskii (KTB)" phase transition [48]. It manifests itself in the conductance as a threshold and the current voltage relation obeys

$$I \propto V^{\zeta(T)},$$

where $\zeta(T)$ is a temperature dependent exponent.

Tighe et al. [87] made the same measurements and found a contradictory result, in which the I-V curve data could be better described by an Arrhenius form, instead of a KTB transition.

The early theoretical work on the transport in arrays was done by Geigenmüller [29] and Schön [79]. For two dimensional arrays of metallic islands, they found that the I-V curve has a threshold voltage which is proportional to the linear array size N.
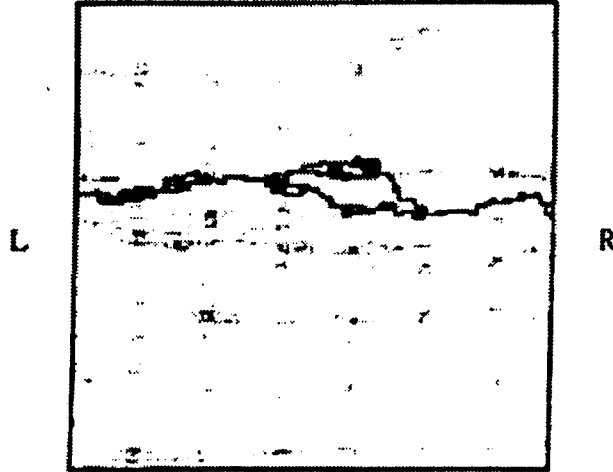
Figure 1.6: Formation of current carrying paths (From Ref. [72]).

Another study has been done by Middleton and Wingreen [72] in the presence of disorder. They also found the same linear dependence on N. The authors incorporated the disorder into the model by assuming that each island, i, has an offset charge, q_i, such that $0 \leq q_i \leq e$. They first calculated the current in a one dimensional array as a function of the voltage. The current is zero up to a voltage V_T and when $V > V_T$, I increases with exponent $\zeta = 1$. Near the threshold, the current voltage relationship is then:

$$I \sim (V - V_T)^\zeta. \tag{1.6}$$

In a two dimensional array, very near threshold, the current flows in a single narrow channel. When the voltage is increased, multiple branching channels are formed (Fig. 1.6). The exponent ζ can be calculated by finding the parallel channel separation $\xi_\perp \sim v^{-2/3}$, and therefore the density of channels $N/\xi_\perp \sim v^{2/3}$. Here v denotes $(V - V_T)/V_T$. Since the current for a single channel scales as the first power of the voltage, the overal critical exponent, ζ is 5/3 for a two dimensional array.

The inter-dot electron-electron interactions in arrays have also been studied microscopically using a Mott-Hubbard approach [82].

1.4 Bistability in Low Dimensional Quantum Structures

One of the most important aspects of the data presented in this dissertation is the multi-stability in the I-V curves of the devices. Previous work on similar and possibly relevant multi-stabilities in low dimensional semi-conductors will be reviewed in this section.

1.4.1 Bistability in Resonant Tunneling Devices

Resonant tunneling of electrons through structures consisting of a quantum well confined by two penetrable barriers provided one of the first observations of two dimensional electronic states in semiconductor heterostructures. A typical I-V curve of such a Double Barrier Resonant Tunneling Structure (DBRTS) shows an "N-Type" negative differential resistance (NDR). In 1987, Goldman and Tsui reported the I-V characteristics of a DBRTS which exhibited intrinsic bistability [31]. An experimental result is shown in Fig. 1.7.

The instability is due to the space-charge formed in the well. Once an electron tunnels into the well, it occupies a resonant state with kinetic energy E_0. The lifetime τ of this electron in the well is $\tau \simeq \hbar/T_2 E_0$. Here T_2 denotes the transmission coefficient of the collector barrier. Since the flux Φ_c of electrons passing through the well in the steady state is J, the sheet density σ of electrons in this accumulation layer is $\sigma = \tau J \simeq \hbar J/T_2 E_0$. Consequently, the electric field in the collector barrier V_2/d is significantly greater than that in the emitter barrier, V_1/d. From Gauss' law,

$$V_1 = V_2 - (4\pi/\epsilon)d\sigma \simeq V_2 - (4\pi/\epsilon)d\hbar J/T_2 E_0, \qquad (1.7)$$

where ϵ is the static dielectric constant of *GaAs*. The voltage drops across the different regions of the structure must add up to V. Therefore, both V_1 and Δ_1 (the depth in
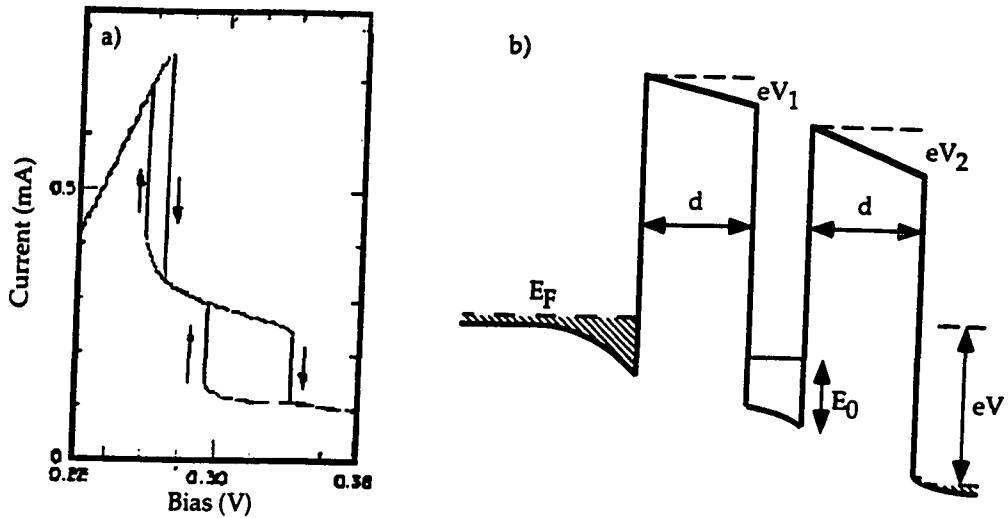
Figure 1.7: The I-V curve of a DBRTS (From Ref. [31]).

energy of the accumulation layer in the emitter), decrease (at fixed V) as J increases. Since J explicitly depends on V_1, T_1 and Δ_1, two stable current states occur at certain biases, causing the hysteresis [31]. The hysteresis can be enhanced by increasing the collector barrier thickness, which gives a larger τ.

1.4.2   Negative Differential Conductance in a Semiconductor Superlattice

Another interesting system which exhibits negative differential conductance (or resistance) is the semiconductor "superlattice", a $GaAs/AlGaAs$ periodic structure. In 1974, Esaki and Chang reported a device in which the differential conductance first decreases, followed by a rapid drop to negative values, then, at high fields, exhibits an oscillatory behavior with respect to the applied voltage [22]. The period coincides with the energy difference between quantized states or bands. Fig. 1.8 illustrates the differential conductance as a function of the applied field at various temperatures. At very low voltages, the current is dominated by band conduction Fig. 1.8(a). For higher voltages, the conductance drops rapidly which can be interpreted as the spontaneous
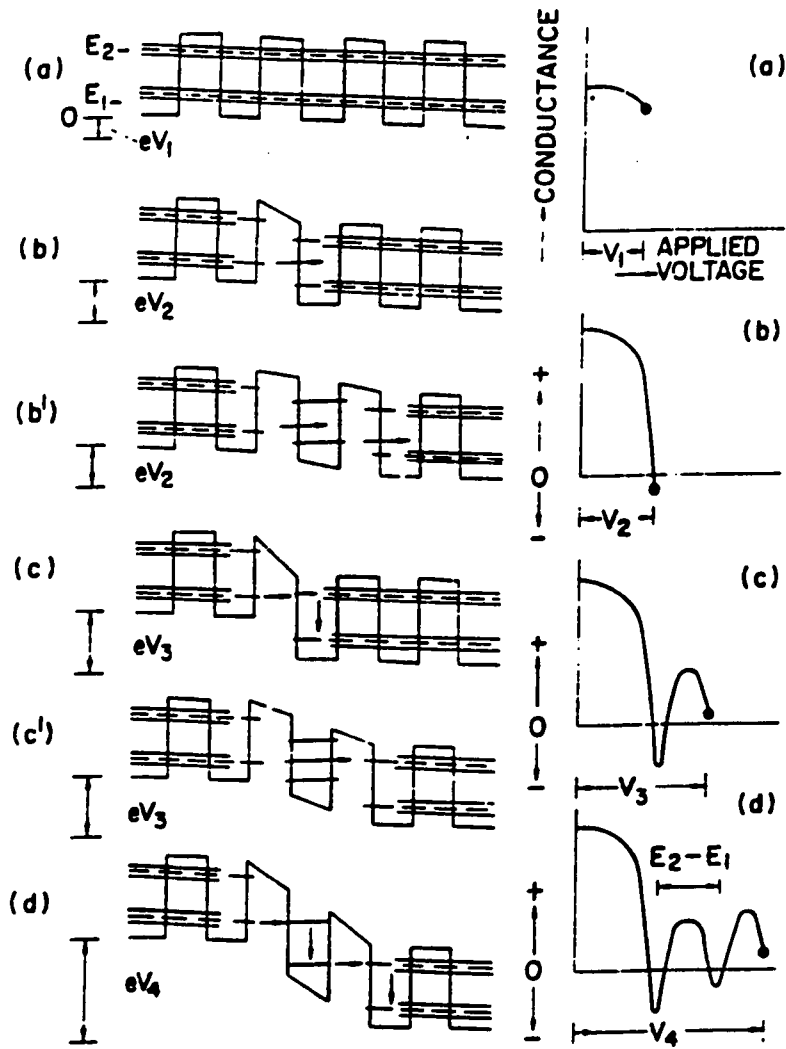
Figure 1.8: The domain formation in a superlattice (From Ref. [22]).
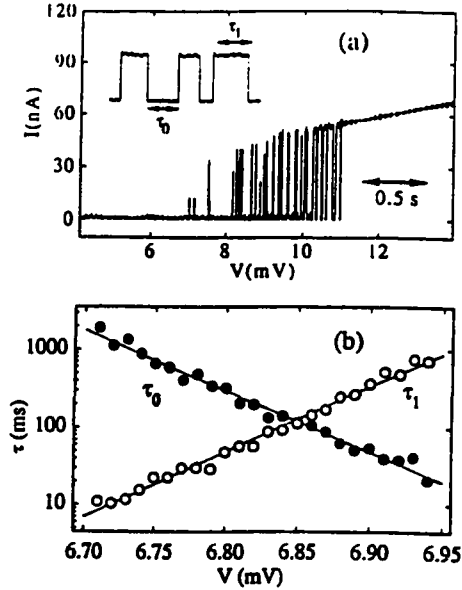
Figure 1.9: The random telegraph signal in etched barriers (From Ref. [76]).

generation of a high field domain (Fig. 1.8(c)). This high field domain formation is an inherent feature of the voltage-controlled negative-conductance medium [86], and dominates the total transport characteristics of the whole system. Further details about this system is described in Ref.s [23, 22].

1.4.3   Transport Through a Submicron Lateral Barrier

Pilling et al. have recently investigated the nonlinear transport through a submicron lateral barrier [76], produced by a shallow etch in a 2-DEG structure. After illumination, the I-V curve contains a region of bistability. The current in this region exhibits a random telegraph signal. The voltage dependence of the characteristic (mean) time constants τ_1 and τ_0 for the respective conducting and insulating states are shown in Fig. 1.9, together with a slow sweep of the voltage. The time constants vary exponentially with the source drain voltage. The hysteresis loops are seen when the time constants at the crossing point ($\tau_0 = \tau_1$) are much larger than the measurement time. The same group observed hysteresis in devices etched deeper than the 2-DEG which

clearly means that the electron wavefunction, in this case, extends into the substrate.

1.4.4   Hot Electron Bistability

The last experiment described in this section is the recently reported single dot Hot Electron Bistability measuremets, by Wu et al.[94]. The authors measured an S-type Negative Differential Conductance (NDC) in a split gate lateral double constriction device. They suggested a mechanism similar to the one proposed by Hess et al. [39]. According to this mechanism, when the source-drain voltage is increased, the number of electrons injected over the first barrier increases, and the electrons are injected into the well with increasing amounts of kinetic energy. This excess kinetic energy is lost through collisions with cold electrons in the well, therefore raising the average temperature of the electrons inside the well. At a critical current density, thermionic emission of hot electrons across the second barrier increases dramatically, giving rise to the NDC.

To interpret the above experimental results, a theoretical study was made by Goodnick et al. [32]. This model will be described in more detail in Sec. 5.3.

Chapter 2

Device Fabrication and Experimental Setup

2.1 Introduction

With recent developments in Molecular Beam Epitaxy (MBE) technology, it has become possible to fabricate high quality two dimensional electron systems. A particularly attractive structure is the $GaAs/Al_xGa_{1-x}As$ Modulation Doped Heterostructure in which $4.2K$ electron mobilities up to $10^7 cm^2/Vs$ were reported [77]. Because of its high purity, this system is very suitable for the study of ballistic electron effects [10], quantum coherent effects [10], and electron-electron interactions as observed in fractional quantum hall effect (FQHE) [77]. Since the observation of single electron charging in silicon quantum wires [80], modulation doped heterostructures have also been extensively used to study single electron effects controllably.

A well established method for fabricating quantum dots in these structures is electron beam lithography and subsequent gate metal deposition (lift-off). A particular device is the split-gate quantum dot in which separate negative voltages are simultaneously applied to the gates to deplete the surrounding semiconductor regions to form the dot and set the transparencies of the tunnel barriers [49]. Although nanoscale gate deposition by lift-off is a very powerful method for the confinement of electrons in single dots, it becomes vastly harder to handle and characterize the devices as

the number of gates increases. This makes it impossible to use split-gates to control individual elements in a large array. Therefore, in the 200 × 200 arrays studied in this thesis, e-beam patterned etching is used with a single to form the dots. Since the same gate also adjusts the coupling between the individual array elements, there is somewhat less control than in the split gate structures.

In this chapter, the MBE growth parameters and conditions of the wafers will first be presented in detail. Next, the electron beam lithography, etching and optical lithography steps will be described. In the last section, the measurement setup will be explained.

2.2 Molecular Beam Epitaxy (MBE) Growth

The details about the general principles of MBE can be found in [16, 34, 38, 55]. All the two dimensional electron gas (2-DEG) wafers used in this work were grown in a Varian GENII MBE system. The growth procedure is as follows: The semi-insulating *GaAs* substrate is placed in the growth chamber after being baked at $400C$ for one hour. Then the *Al* and *Ga* furnaces are heated up to $1350C$ and $1004C$ respectively. These temperatures are chosen using the calibration curves such that the ratio of the growth rate, *gr* for *Ga* and the rate for *Al* is close to $0.66/0.34$ ($x = 0.34$). The 34% *Al* presence in the $Al_xGa_{1-x}As$ layer gives a large conduction band discontinuity, which facilitates the formation of the 2-DEG. x must be kept lower than 40% to ensure that the minimum of the conduction band in the *AlGaAs* layer is in the Γ valley [1]. The growth rates corresponding to these temperatures are $0.575\mu m/hr$ for *Ga* and $0.297\mu m/hr$ for *Al* giving $x = 0.34$ as desired.

Next, the *As* furnace is heated up to $323C$ such that the environment is *As* rich. The *As* flux was set to be at least 15 times larger than the total of *Ga* and *Al* fluxes. This ratio is kept lower than 22 for lower defect density. The *Si* temperature was set to $1318C$ to give a doping density N_D of $4.2 \times 10^{18}/cm^3$ assuming a doped $Al_{0.34}Ga_{0.66}As$ layer thickness of 170Å. The dopant flux, Φ_{Si} is found from the relation

$$\Phi_{Si} = N_D \times gr. \tag{2.1}$$
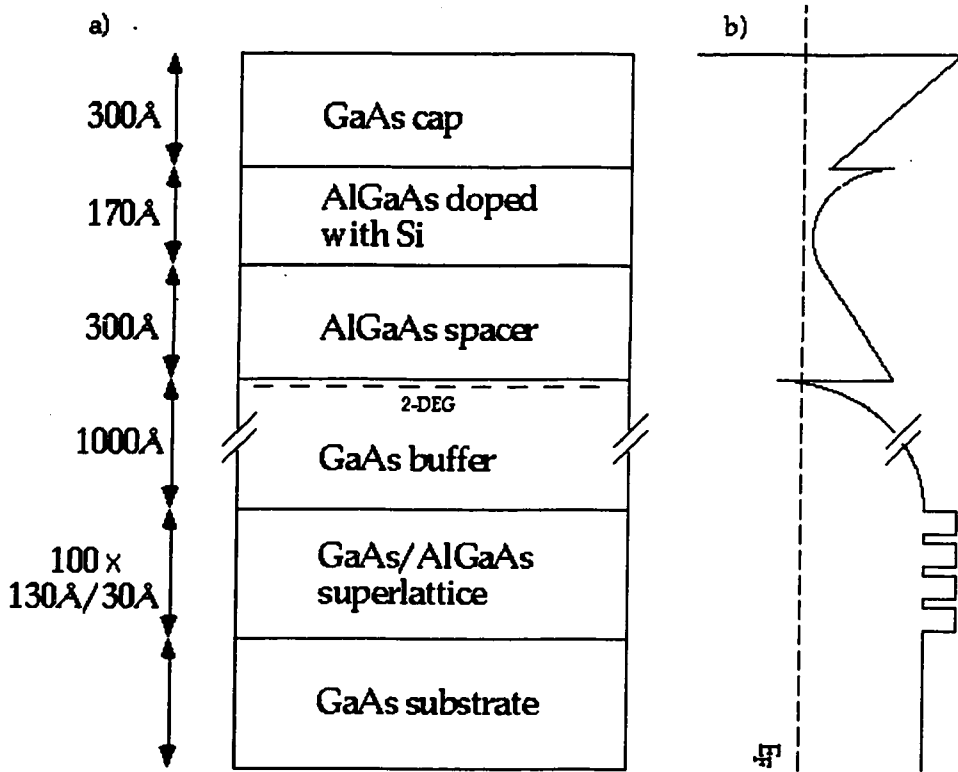
Figure 2.1: a) The schematic diagram showing the layer thicknesses of the 2-DEG wafers (not to scale). b) The corresponding band diagram.

When all the sources become stable at their respective growth temperatures, the growth can be started by opening the As shutter and heating the substrate up to $700C$ to desorb the oxide. The substrate temperature is then set to $640C$. This value has been found to be the optimum for high mobility structures from previous growths. Next, the Ga shutter is opened to grow a $3000\text{\AA}$ $GaAs$ buffer layer (Fig. 2.1). Following the buffer, there is a $GaAs$, $Al_{0.34}Ga_{0.66}As$ superlattice, with a period of 100. Each period consists of a $30\text{\AA}$ $GaAs$ and a $100\text{\AA}$ $Al_{0.34}Ga_{0.66}As$ layer. This superlattice is known to clean up the system by trapping impurities, especially carbon. The buffer ends with an additional $500\text{\AA}$ thick layer of $Al_{0.34}Ga_{0.66}As$. The Ga shutter

is then kept open to grow $1\mu m$ *GaAs*. Then all the shutters, except *As*, are closed for 5 seconds, which is called "growth interrupt". This is a very important interface since after the growth of the rest of the structure, the 2-DEG will be formed here. The growth interrupt gives the atoms enough time to redistribute themselves, making the interface uniform and smooth. On the other hand, too long a break during the growth results in excess contamination, hence decreases the mobility. Therefore, there is an optimum interrupt time, 5 seconds in this case, usually found from previous growths. The next layer is the "spacer" which separates the ionized donors from the 2-DEG and enhances the mobility. In the wafers used for this study, the spacer is $300\text{\AA}$ thick and consists of undoped *AlGaAs*. After the spacer, the *Si* shutter is also opened in addition to the *Ga* and *Al* shutters. This way, the *AlGaAs* layer becomes *Si* doped. Finally, there is a $300\text{\AA}$ *GaAs* "cap" layer, which protects the rest of the structure against oxidation.

Several 2-DEG structures were grown with the above procedure. Depending on the condition of the MBE machine, their electron mobilities ranged from $100,000cm^2/Vs$ to $700,000cm^2/Vs$ at $4.2K$. The mobility of the 2-DEG used to make the arrays was $200,000cm^2/Vs$. The growth files for the devices mentioned in the dissertation are given in Appendix B.

2.3 Device Processing

2.3.1 Electron Beam (e-beam) Lithography

The grown wafers were cleaved into square pieces with dimensions $1.3\times1.3cm^2$. Next, 4% PMMA in Chlorobenzene was spun on at $5000rpm$. The resultant thickness was about $1000\text{\AA}$. The pieces were then baked overnight inside a $90C$ oven. They were exposed in a HITACHI e-beam machine, with $450\mu C/cm^2$ dose and developed in 1:2 MIBK: Isopropanol solution for 45 seconds. The exposed and developed regions were then etched by dipping the sample in a 50:5:2 Isopropanol: Phosphoric Acid: Hydrogen Peroxide solution held at $12C$, using an iced water bath. The etch rate was about $25\text{\AA}/sec$ and the etch time was 40 seconds. The resulting etch depth was

$1000\mathring{A}$, deeper than the 2-DEG depth ($770\mathring{A}$). Therefore there is no 2-DEG in the etched regions.

2.3.2 Electron Beam Pattern

The pattern that the HITACHI e-beam machine wrote was generated using DW2000 software, in the GDSII format. It consists of plus sign shaped regions repeated with a period of $0.8\mu m$ in both x and y directions. The defined line thickness of each arm of the plus sign is $100nm$, but for these feature sizes, the actual line thickness is determined by the e-beam spot size and the number and separation of e-beam passes. In other words, a single line of zero thickness drawn by a single pass e-beam exposure would be the same line as a $100nm$ thick defined line exposed by a single pass of the beam.

In addition to the repeated shapes, there are isolation lines which electrically isolate one side of the array from the other and the control device from the array. This can be seen clearly in Fig. 2.2 a). All the cross hatched regions in this figure are etched away, therefore they don't contain any 2-DEG at any applied voltage. The e-beam pattern also has larger alignment marks with $10\mu m$ feature size, so that the etched pattern can be easily aligned with the optical masks.

The results presented in Chapters 3 and 4 were obtained from four different devices. The lithographic distance, d, shown in Fig. 2.2 is $450nm$, $400nm$, $350nm$, and $300nm$ for these arrays and they will be referred to as *Device 1*, *Device 2*, *Device 3*, and *Device 4* respectively. SEM photos show that, due to etching in the lateral direction, d', which is the separation of plus signs after processing, is about $100nm$ shorter than d in the e-beam pattern.

2.3.3 Optical Lithography

After e-beam lithography and etching, three standard optical lithography steps were performed. First, the devices were isolated by mesa etching. The etch consisted of 1:1:30 H_3PO_4:H_2O_2:H_2O solution. Next, $Au_{88}Ge_{12}$(eutectic)$/Ni/Au$ ohmic contacts were deposited in an e-beam evaporator and lifted off. The thicknesses of the above
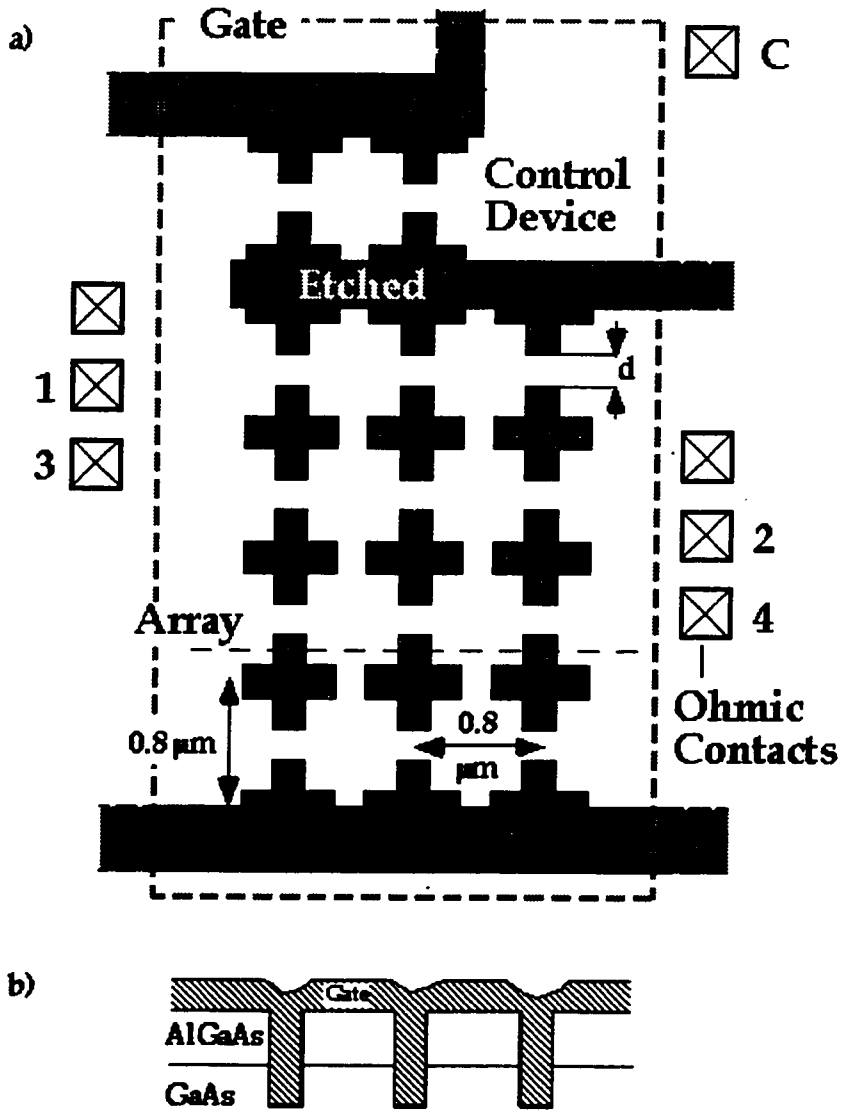
Figure 2.2: a) The symbolic diagram for the layout of the device (not to scale). b) The cross-section along the dotted line in a).

layers are 250$\overset{\circ}{A}$, 150$\overset{\circ}{A}$, 2200$\overset{\circ}{A}$ respectively. Finally, a Cr/Au 100$\overset{\circ}{A}$/1000$\overset{\circ}{A}$ gate metal was deposited covering the whole mesa including the array and control device. All the optical and e-beam processing patterns generated in the DW2000 and the SEM photo of the corresponding device are shown in Fig. 2.4 and Fig. 2.3 respectively. In the photo, the upper left corner is *Device 1* (Fig. 2.5), and the lower left corner is *Device 4* (Fig. 2.6). A control device is shown in Fig. 2.7.

2.4   Measurement Setup

Fig. 2.8 shows the measurement setup used to characterize the electrical transport properties of the arrays. They were measured in a dilution refrigerator at mixing chamber tempearture from 20 to 700mK. A *dc* voltage bias which could be swept, plus a 10μV, 11.4Hz *ac* voltage bias were applied across the array. The swept *dc* signal was generated by SRS DS335 signal generator functioning in the very low frequency (typically 0.0001Hz) triangular wave mode. The *ac* signal was the output of an EG&G lock-in amplifier. The two signals were fed into the differential inputs of a voltage sensitive preamp (SRS SR560), added with unity gain and the (50Ω) output was connected to one of the ohmic contacts[1] (1 in Fig. 2.2).

The voltage drop across the array (V_{arr}) was measured using two other ohmic contacts (3 and 4 in Fig. 2.2). The *dc* part of the voltage was directly measured with an HP34401A voltmeter whose digital output was connected to the computer. The *ac* part of the voltage was connected to the input of the lock-in (EG&G), and the output of the lock-in was measured with another HP34401A voltmeter.

The current (I_{ds}) was measured by connecting the ohmic contact on the opposite side of the array (2 in Fig. 2.2) to a current sensitive preamplifier. In most of the measurements, a built in PAR181 current sensitive preamplifier was used. The *dc* part of the current was taken to a HP34401A voltmeter from the monitor output of the current sensitive preamplifier. The *ac* signal was fed into the input of a second lock-in whose output was connected to a digital voltmeter. The *ac* lock-in

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[1]One of the contacts on the other side of the array is connected to a current sensitive preamplifier creating a virtual ground.
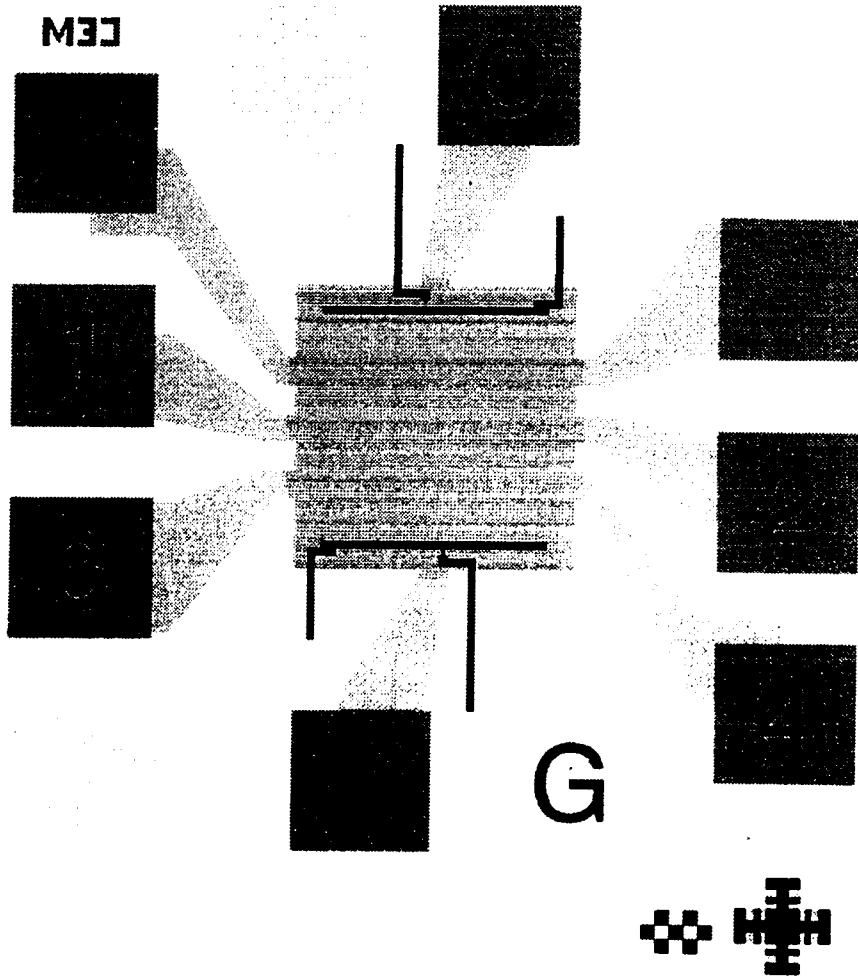
Figure 2.3: The schematic diagram of the device, as drawn in DW2000.The light grey region is the mesa. The darker region is the gate. The dark grey squares are the ohmic contacts. The black lines show the regions to be exposed by the e-beam. Between the two horizontal lines is the array (The plus signs are too small to see in this scale). The vertical lines isolate the array and the control devices. The latter are located at the intersection of the central vertical lines and the horizontal lines. The shapes at the lower right corner are the alignment marks.
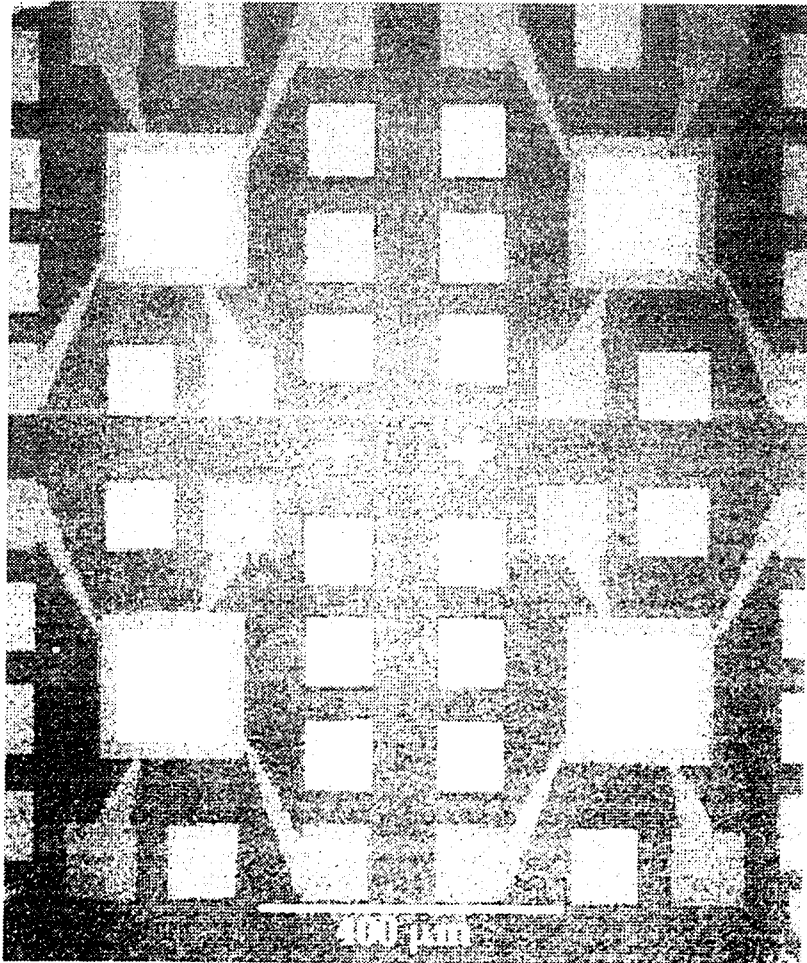
Figure 2.4: SEM photo of four finished devices. The lighter regions in the middle with diagonal lines contain the plus signs. They look this way because of interference.
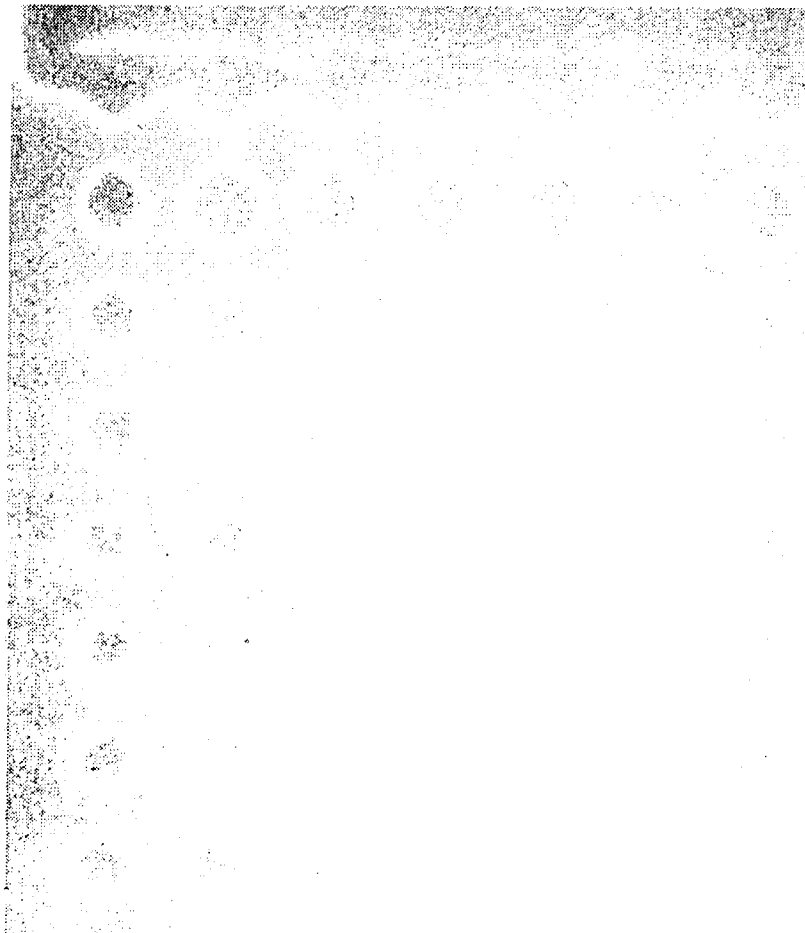
Figure 2.5: SEM photo of *Device 1*. Because of wet etching, the corners become smooth and for this device the plus sings look almost circular.
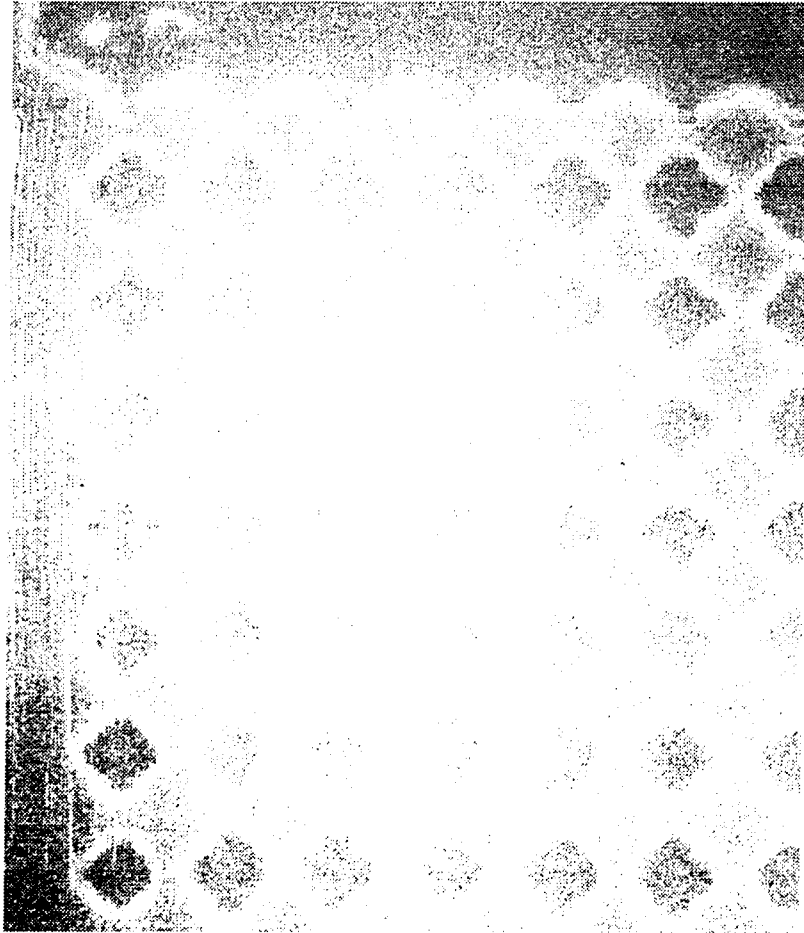
Figure 2.6: SEM photo of *Device 4*.
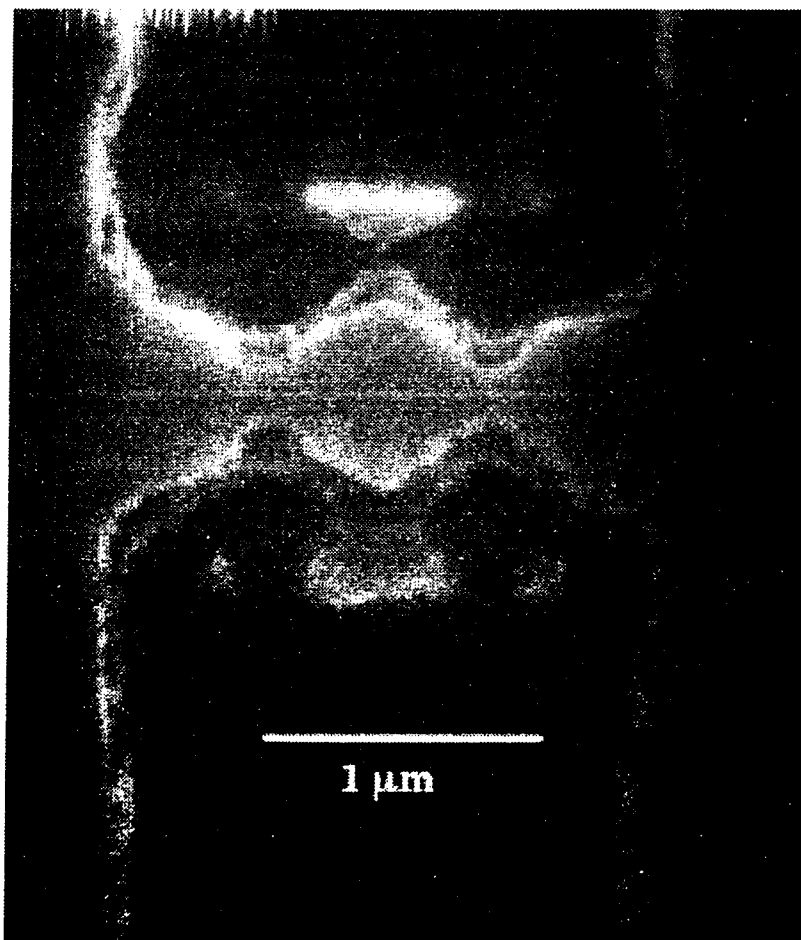
Figure 2.7: SEM photo of the Control Device.
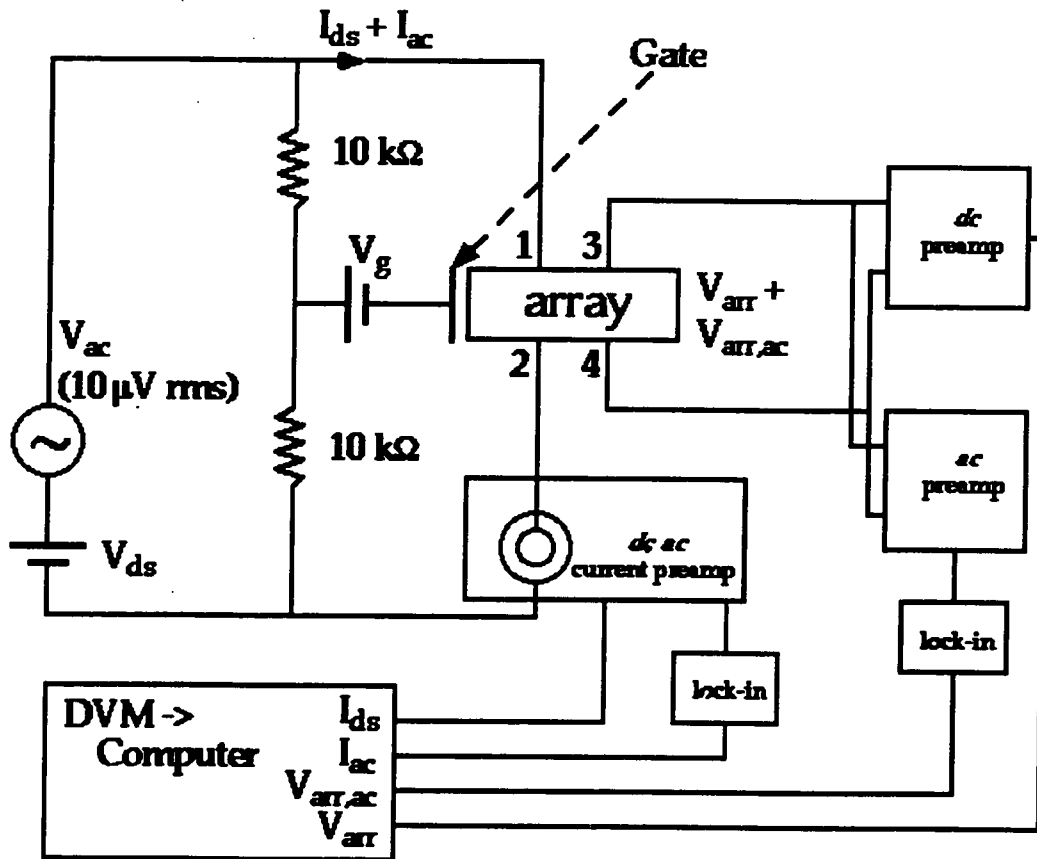
Figure 2.8: The measurement setup.

measurement directly gives the differential conductance, dI_{ds}/dV_{arr}, as a function of V_{arr}. In practice, however, the *dc* I-V measurements were quite clean and sufficiently characterized the observed behavior.

The gate voltage (V_g) was applied from a battery box. It was referenced to the midpoint of the source-drain voltage by means of two $10k\Omega$ resistors. During the measurement, the voltmeter which measured V_g was turned off to minimize the noise. For the arrays, if the gate voltage is referenced to ground, the switching and hysteresis can only be observed on one side of the I-V curve. If it is referenced to the midpoint of V_{ds}, the curve is relatively symmetric. The array voltage $|V_{arr}|$ around which the first loop appears, is of the same order on both negative and positive sides of the curve (Fig. 3.11). The details of the hysteresis and switching, however, appear to be different.

In the case of a single dot, switching and hysteresis is observed on both sides of the curve at similar $|V_{arr}|$, even if V_g is referenced to ground.

Chapter 3

Experimental Results

3.1   Introduction

In this chapter, the main experimental results will be presented[1]. First, the general I-
V curves of the arrays, their temperature, gate voltage and magnetic field dependence
will be described. Next, the I-V curves of the control devices will be discussed [21, 81].

3.2   Array Characteristics

3.2.1   Gate Voltage Dependence

Fig. 3.1 shows general I-V curves of *Device 2*, as a function of gate voltage, V_g, at $T =$
$20mK$. These curves illustrate typical multiple hysteresis loops as a function of the
inter-dot coupling adjusted by the gate. For $V_g = -98mV$, the I-V curve has a single
loop near $4mV$ bias voltage. As the gate voltage becomes more negative, the width of
this loop increases and a new hysteresis loop appears for $V_g < -106mV$. These two
loops merge at a gate voltage between $-114mV$ and $-118mV$. The corresponding
gate voltage dependence of the hysteresis loop widths is shown in Fig. 3.2, together
with the best fits to the data points (See 5.6).

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[1]As noted in the Abstract, all the results in this chapter are from devices etched $1000\mathring{A}$ deep,
and referred to as *Device 1, Device 2, Device 3* and *Device 4*.
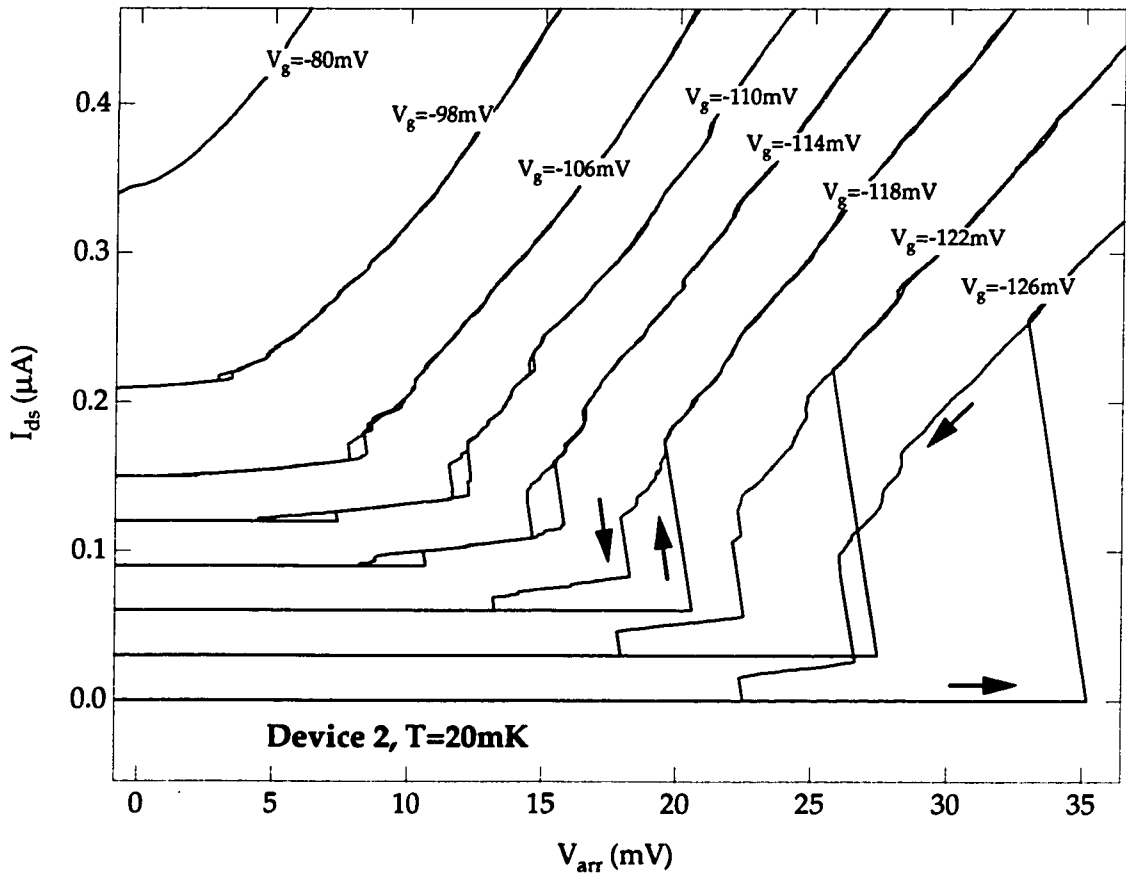
Figure 3.1: The I-V curves of *Device 2*. The curves are offset in proportion to the gate voltage for clarity.
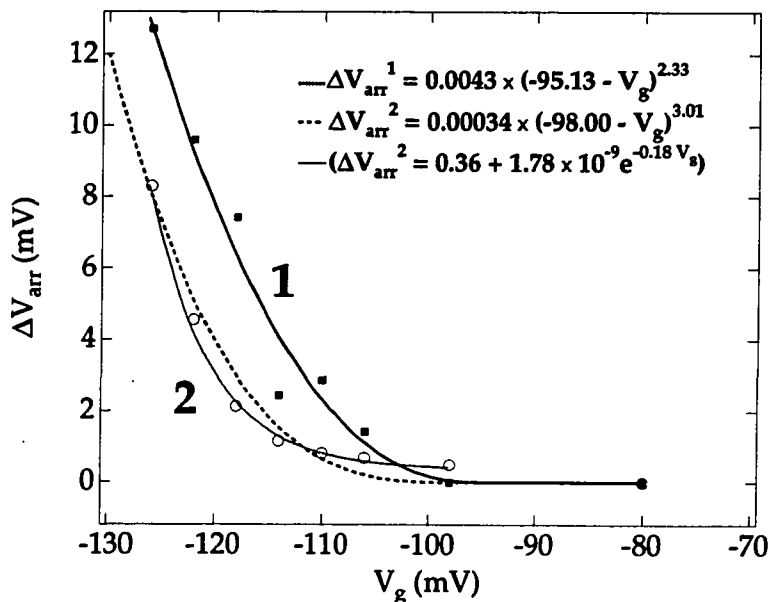
Figure 3.2: Gate voltage dependence of the hysteresis width.

Fig. 3.1 also illustrates the discontinuous jumps in the current (within the resolution of a single data point), which will be referred to as "switching events". In the curves for $Vg < -118mV$, multiple switching events occurring in a single loop can be noticed very clearly. In all hysteresis loops observed, the switching-on voltage for increasing V_{arr} is larger than the switching-off voltage when V_{arr} is decreased; that is, all hysteresis loops are counter-clockwise in I versus V. We also find counter-clockwise sub-loops on both the upper and lower parts of the curve if the sweep direction is reversed following a current jump. This "hierarchy of hysteresis loops" will be discussed in more detail in the next subsection.

Fig. 3.3 shows the I-V curves of *Device 3*, for three different gate voltages at $T = 20mK$. The general qualitative behavior is the same as that of *Device 2*. The details of the hysteresis loops, however, are different. For $V_g = -37mV$ several small loops can be noticed. These loops combine into two bigger ones when the gate voltage is decreased to $-40mV$. At $V_g = -43mV$ these two loops also merge and form the large loop seen in Fig. 3.3.
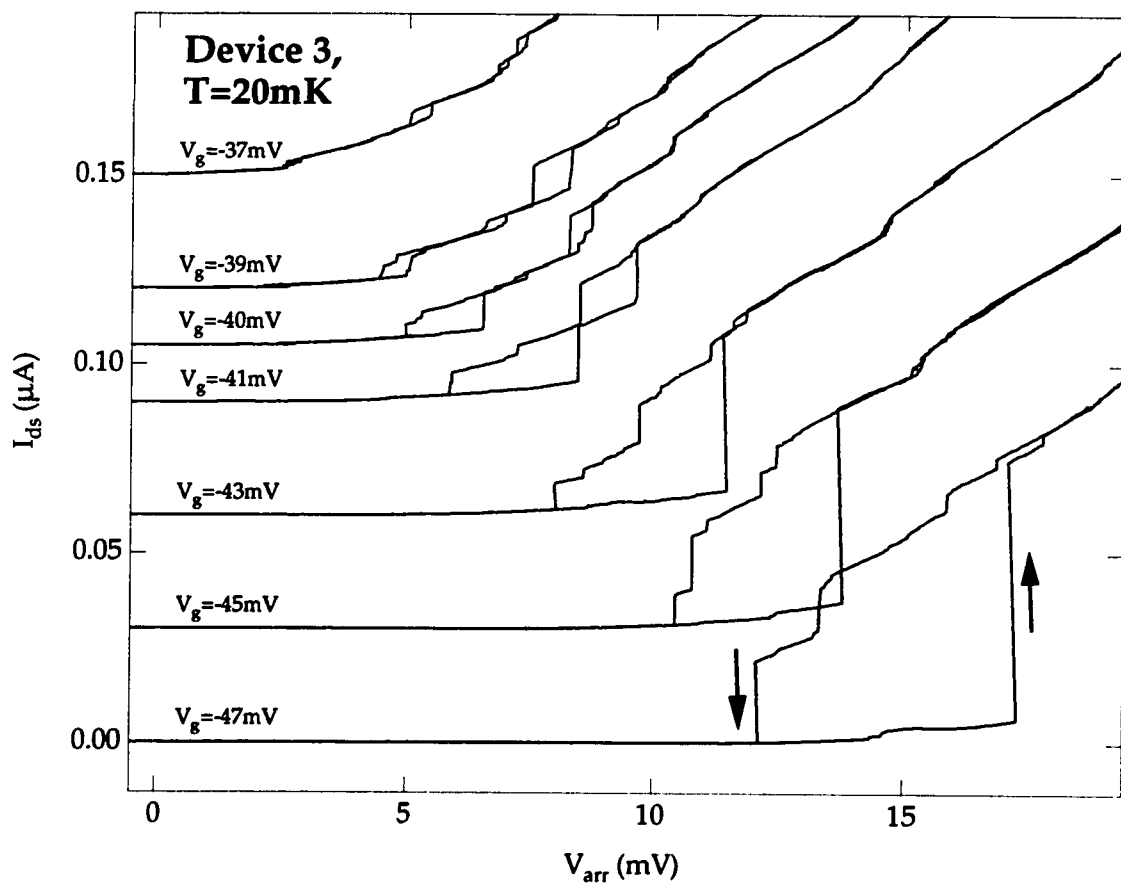
Figure 3.3: The I-V curves of *Device 3*, for various gate voltages.

The I-V curves of *Device 1* are also qualitatively similar to those of *Device 2* and *Device 3*. The enlarged view of the main loop for $V_g = -154mV$ and $T = 70mK^2$ is shown in Fig. 3.4. The negative slope of each switching event results from using two ohmic contacts other than those through which the source-drain voltage is applied, to measure V_{arr}. As soon as a switching event occurs, there is a discrete change in the voltage drop accros the array. This is due to the discrete jump in the current which leads to a discrete change in the voltage dropped on the ohmic contacts through which the voltage is applied. Therefore, the slope gives the total resistance of the ohmic contacts 1 and 2 in Fig. 2.2.

Device 4 was different than *Devices 1, 2* and *3* in that it was already pinched off at zero gate voltage $V_g = 0$ at the base temperature, so no data was taken from it.

The pinch-off voltages[3] for *Device 1, 2* and *3* are $-140mV, -98mV$ and $-37mV$, respectively. This means that the pinch-off voltages depend linearly on the size of the opening between each plus sign (350nm, 300nm and 250nm from SEM pictures).

The device characteristics in $\{I_{ds}, V_{arr}, V_g\}$ space can also be measured by keeping V_{ds} constant[4] and sweeping the gate voltage. Fig. 3.5 shows the data from *Device 3*.

As expected, various hysteresis loops move and merge as V_g is changed.

3.2.2 Hierarchy of Switching Events

Fig. 3.4 shows the details of the main hysteresis loop in the I-V curve of *Device 1*. If the increasing *dc* voltage sweep is stopped at a V_{arr} value very close to $14mV$ (but smaller) and the sweep direction is reversed, it is possible to observe the subloop shown in the inset. There are two additional switching events: One on the lower part and the other on the upper part of the subloop. This means that by reversing the sweep direction, it would be possible to see a hysteresis loop inside the subloop in the inset. It is important to note the current scale for the subloop which is about 50 times smaller than that for the main loop.

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[2]The switching voltages in the main loop for this device are very close to those at $T = 20mK$, at the same V_g. This example is chosen since the subloops and hierarchy of switching events are more noticeable.

[3]The pinch-off voltage is the gate voltage for which $dI_{ds}/dV_{arr} = 0$ at $V_{arr} = 0$.

[4]V_{arr} cannot be kept constant when the measurement configuration in Fig. 2.8 is used.
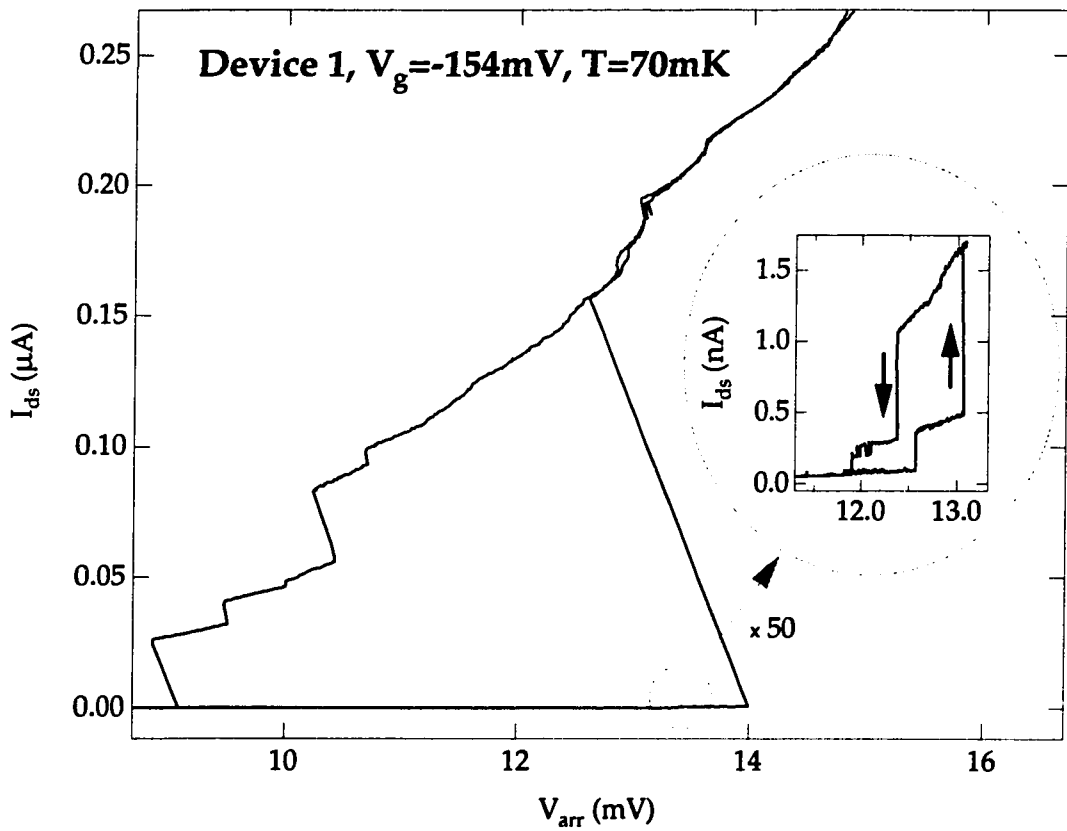
Figure 3.4: The detailed view of a hysteresis loop in the I-V curve of *Device 1*.
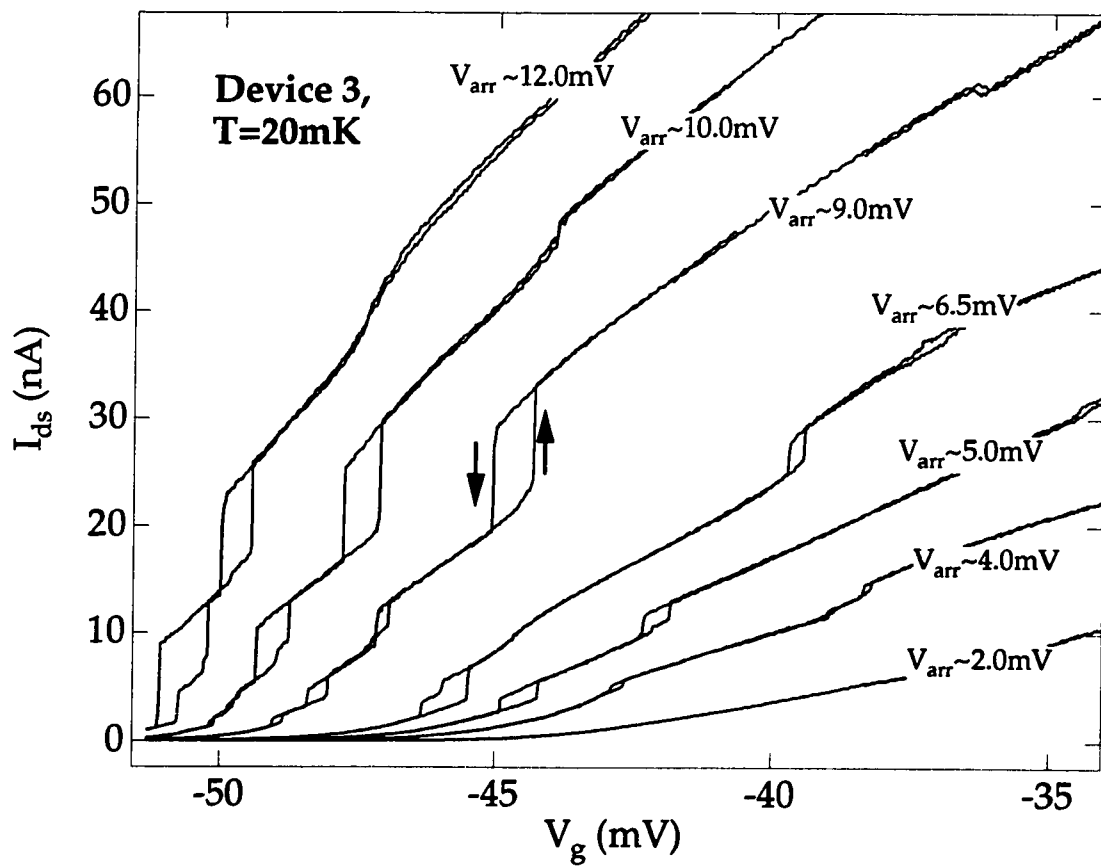
Figure 3.5: The source drain current measured when the gate voltage is swept for a constant drain source voltage V_{arr}

The hierarchy of the switching events can also be observed on the upper part of the I-V curve. Fig. 3.6 shows a hysteresis loop on the upper part of the I-V curve for *Device 3*. The data in this figure was taken as follows: The sweep was started at $V_{arr} = 0$ and the voltage was increased in the positive direction until the main switching event occured. Then the sweep direction was reversed and the voltage was decreased down to $7.0mV$. In this way, the I-V curve was kept in the upper state. Next, the sweep direction was reversed again, increasing the voltage up to $8.25mV$. At this voltage, the sweep direction was reversed one more time, and the loop shown in Fig. 3.6 was obtained. The results show that by reversing the sweep direction, it is possible to observe a hysteresis loop for every single switching event. Although there is a clear hierarchy in the switching events, no obvious rules were observed for the classification of the loops and sub-loops. In other words, it was not possible to construct a self similar hierarchical structure as in fractals. A more detailed study could make it possible to discover such structures.

3.2.3 Temperature Dependence

Fig. 3.7 shows that switching voltages decrease for increasing temperature, and the width of each hysteresis loop also decreases as the temperature increases. It is possible to see in Fig. 3.7 the dissociation of big loops into smaller ones and their disappearance at different temperatures below $680mK$, at which point, hysteresis is no longer observed.

The width of one of the loops is plotted as a function of temperature in Fig. 3.8. A power law fit to this curve gives $\Delta V_{arr} = constant \times (T_0(V_g) - T)^\alpha$. For the main loop in Fig. 3.7, $\alpha = 0.57$ and $T_0 = 663.35K$. This dependence is reminscent of a second order phase transition (See 5.6), the hysteresis width ΔV_{arr} being an order parameter.

There is an apparent tradeoff between the two control parameters V_g and T: at $680mK$, the hysteresis can be recovered if the gate voltage is made $20\text{-}30mV$ more negative (Fig. 3.9). However, the ratio of the loop width to the switching voltage is always smaller than that at $20mK$. This suggests that switching and hysteresis
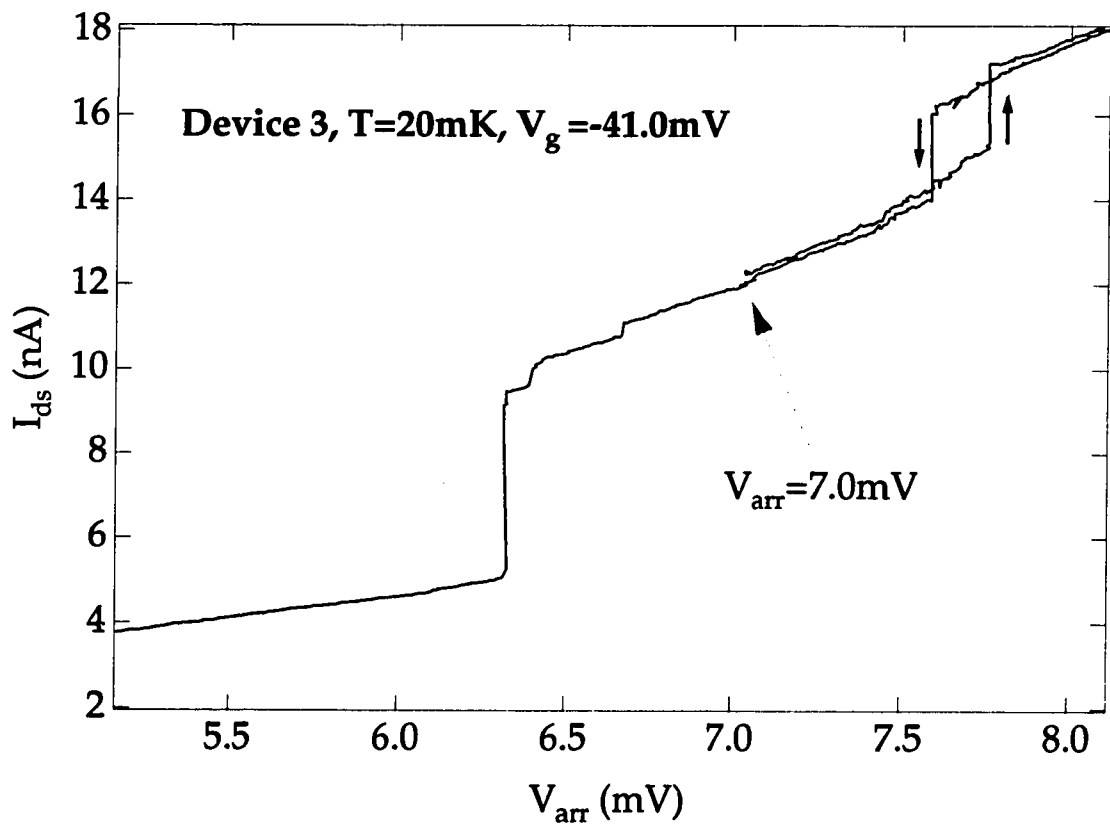
Figure 3.6: Part of the I-V curve of *Device 3* (See Fig. 3.3).
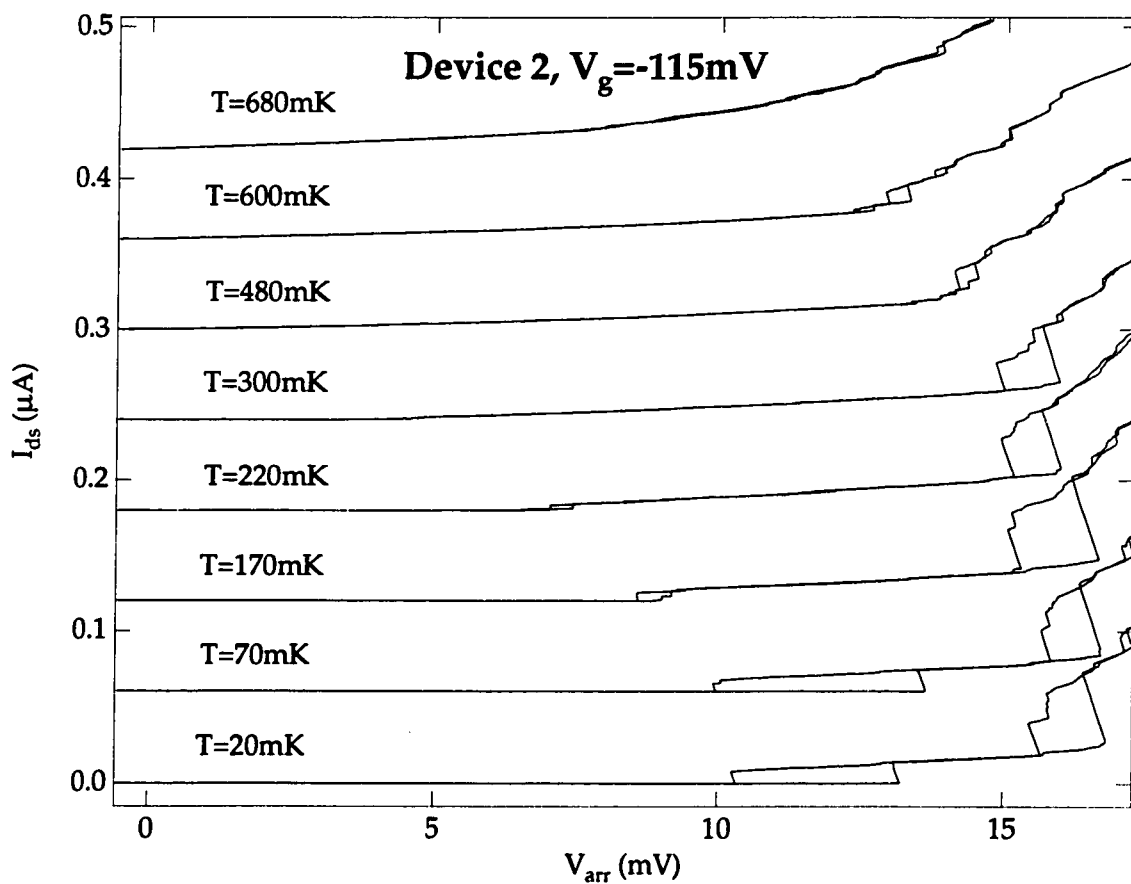
Figure 3.7: Temperature dependence of the I-V curve at a fixed gate voltage (*Device 2*).
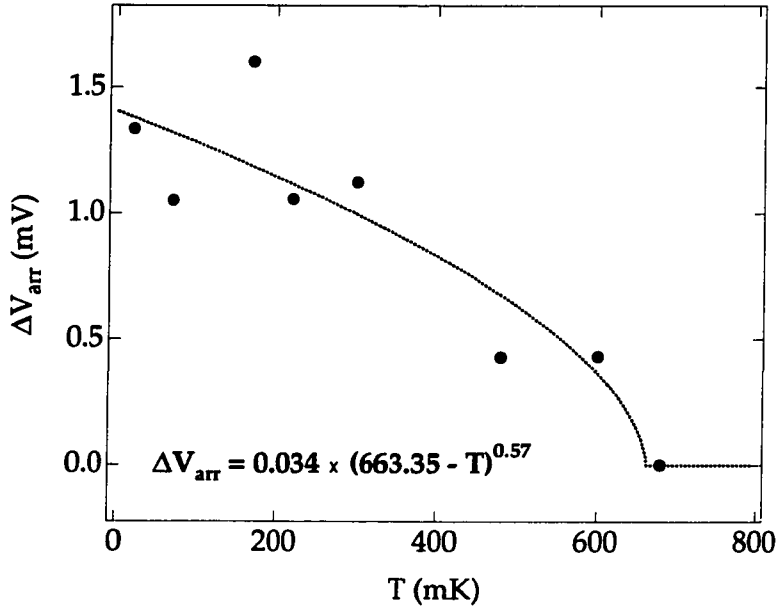
Figure 3.8: Temperature dependence of the hysteresis width of the main loop in the I-V curve of *Device 2*.

will inevitably disappear at sufficiently high temperatures regardless of gate voltage. Indeed, at $4.2K$, no hysteresis is observed in any of the samples.

3.2.4 Current Bias Measurements

By inserting a large resistor (for example $10M\Omega$) in series with the voltage source, a current bias measurement[5] was made (Fig. 3.10). There are multiple voltage peaks in the I-V curve with various heights. This is consistent with the observation of a hierarchy in the switching. The main hysteresis loop is still present in this curve, because the device is voltage biased when it is in the low current state.

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[5]When the device is in an insulating state, its resistance is much more than $10M\Omega$. Therefore, it is current biased only when it has a large enough conductance.
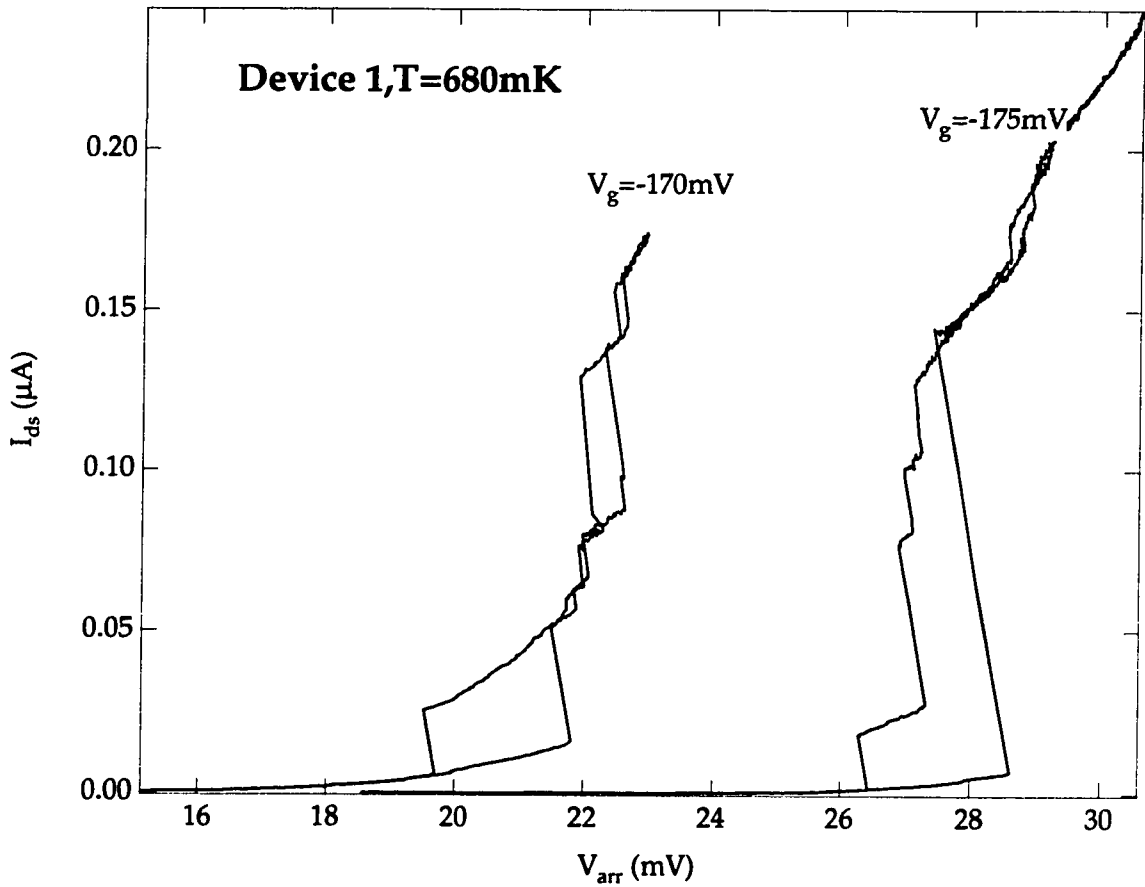
Figure 3.9: The hysteresis recovered at $680mK$, but the width is smaller than that $20mK$ with the same gate voltage.
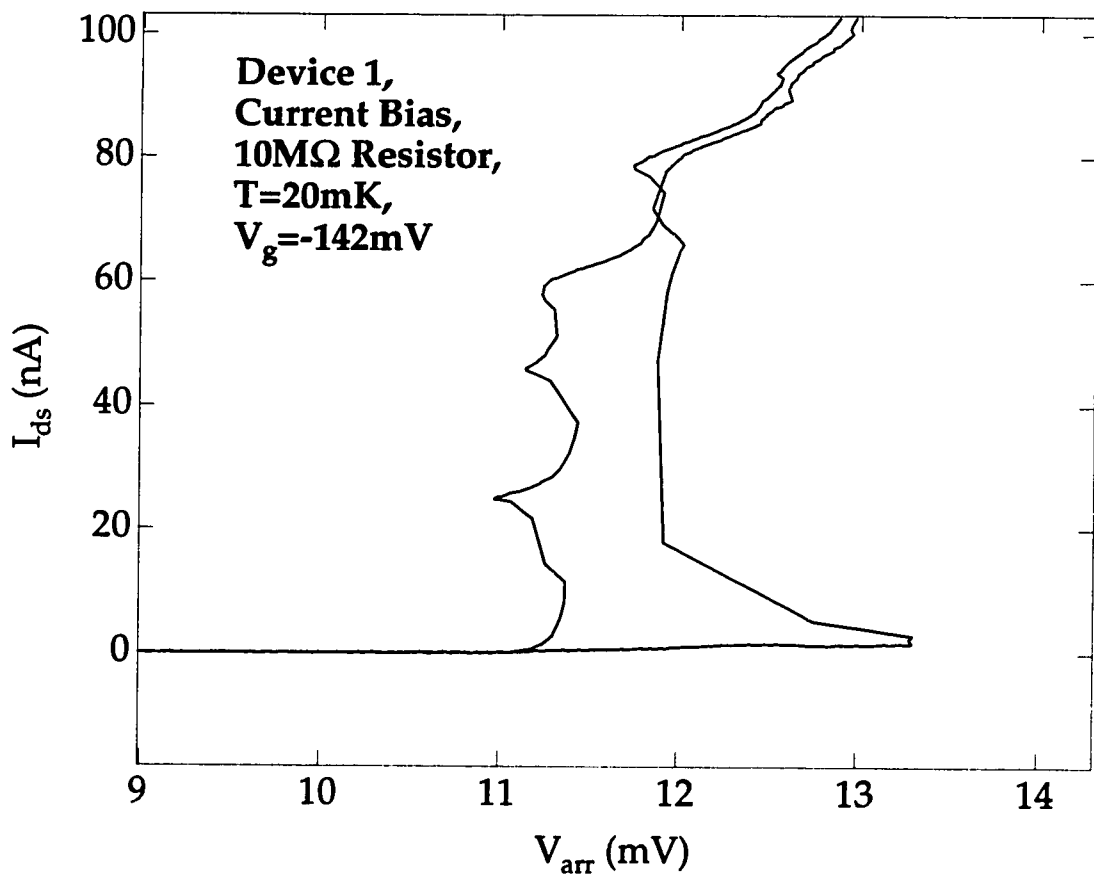
Figure 3.10: I-V curve measured with a current bias.

3.2.5 *ac* Lock-in Measurements

Fig. 3.11 shows the *ac* lock-in measurement data and the corresponding *dc* data for Device 3 at $T = 20mK$ and $V_g = mV$. Multiple hysteresis loops and switching events are also observed in the dI_{ds}/dV_{arr} versus V_{arr} curve. However, because of noise, it is not possible to measure all the switching voltages. Since the *dc* I-V curves had little noise and sufficiently characterized the observed behavior, this will be the only *ac* lock-in measurement result presented in this dissertation.

3.2.6 Magnetic Field Dependence

By studying the magnetic field dependence of the I-V curves, it is possible to make some conclusions about the mechanism for the switching and hysteresis. A magnetic field, B, perturbs the quantum levels and changes their energies. The single electron charging energy, and the electrostatic potential profile, on the other hand, are independent of the field. If the I-V curve depends on B strongly, one can conclude that the observed physics is related to quantum coherence. Otherwise, switching and hysteresis is more likely to be due to a mechanism which is classical in origin.

Fig. 3.12 shows the I-V curves for *Device 3* at various magnetic fields. The main characteristics and the location of the hysteresis loops are independent of the magnetic field. The details of the curves, however, are different especially at large magnetic fields. The conductance of the array is observed to fluctuate. This is consistent with the model in which the Fermi level crosses the localized and extended states as the magnetic field is changed[6] [77].

3.3 Control Device Characteristics

The I-V properties of a single control device Fig. 3.13 located adjacent to the array on each sample were also investigated using the same experimental measurement configuration as for the arrays. In the case of a single dot, we observe no hysteresis near pinch-off, $V_g = -375mV$, however, beyond a gate voltage $20mV$ more negative

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[6]Shubnikov de Haas Oscillations.
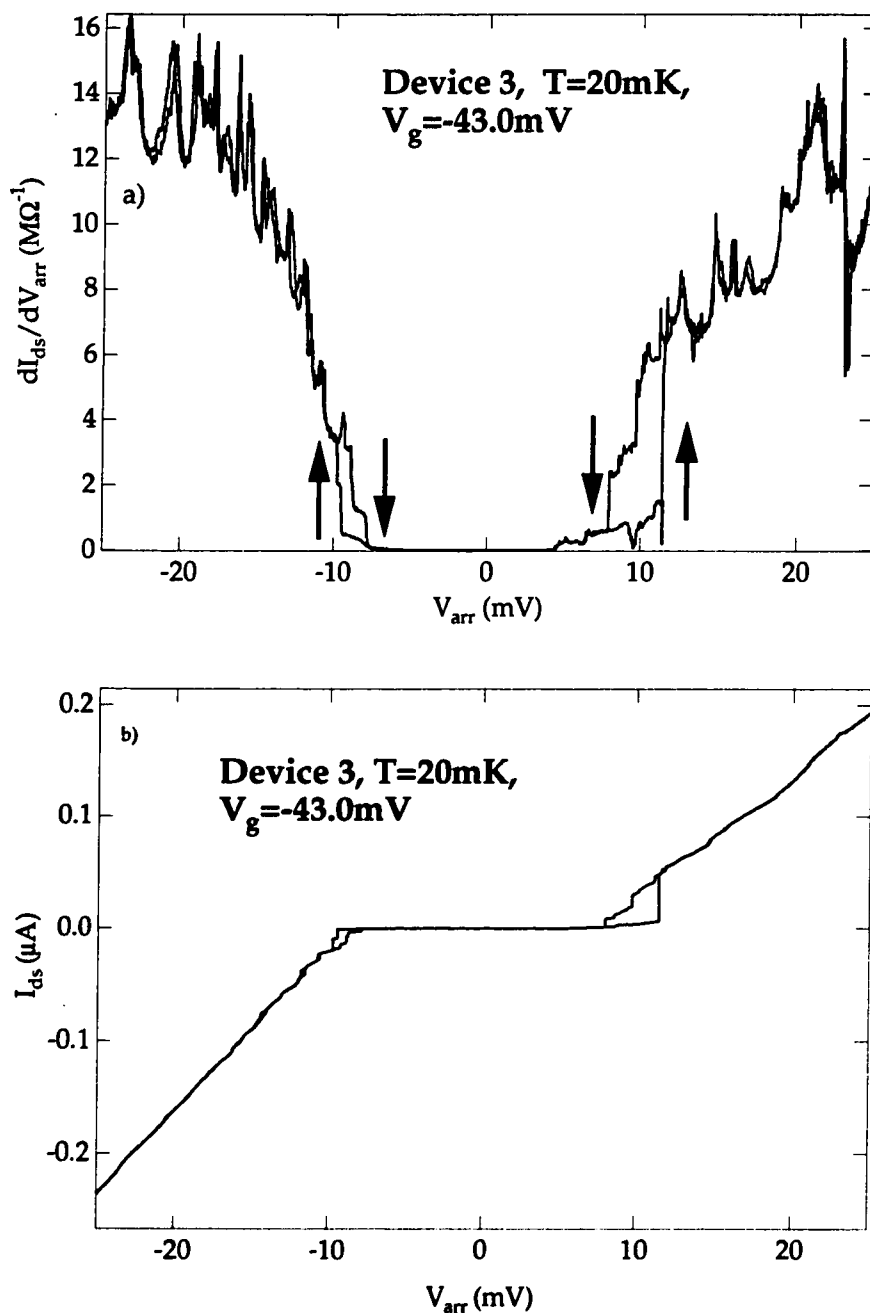
Figure 3.11: a) The differential conductance of the device as a function of V_{arr}. b) The corresponding *dc* I-V curve.
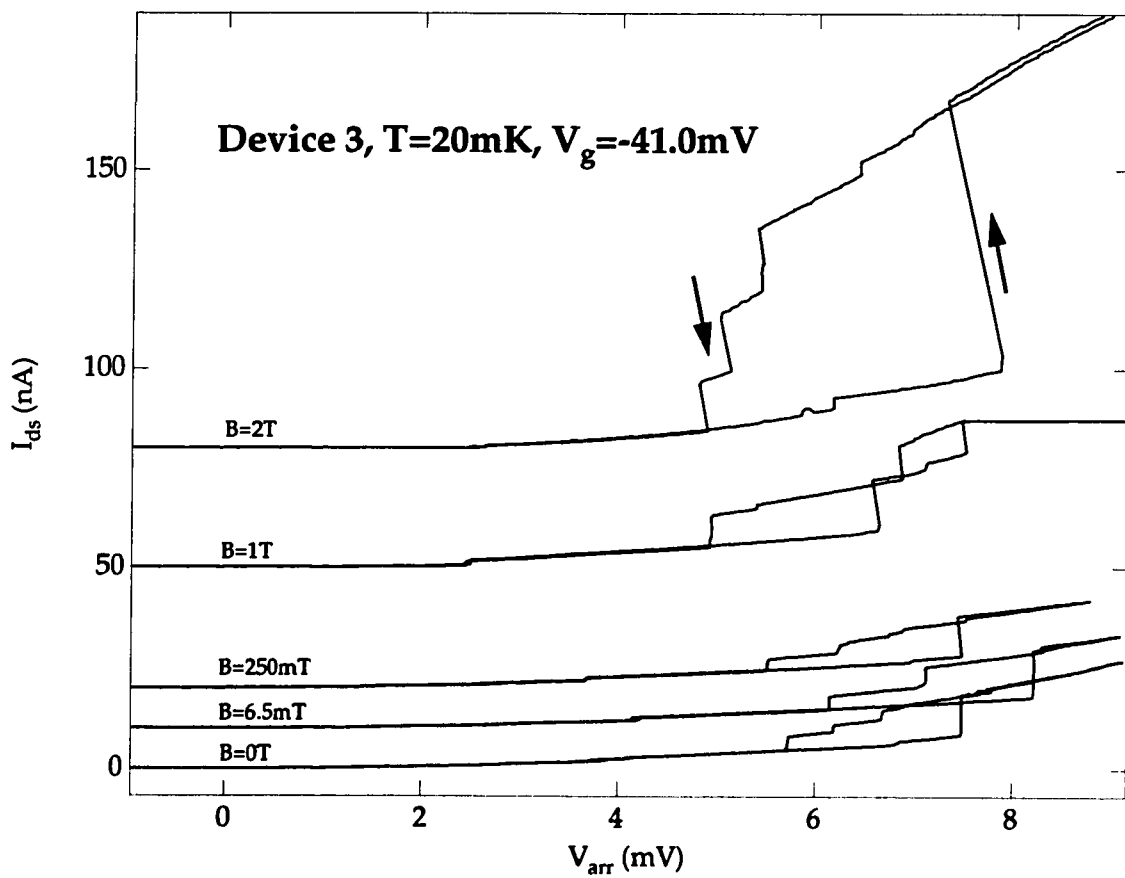
Figure 3.12: The I-V curves of *Device 3* as a function of the magnetic field *B*.
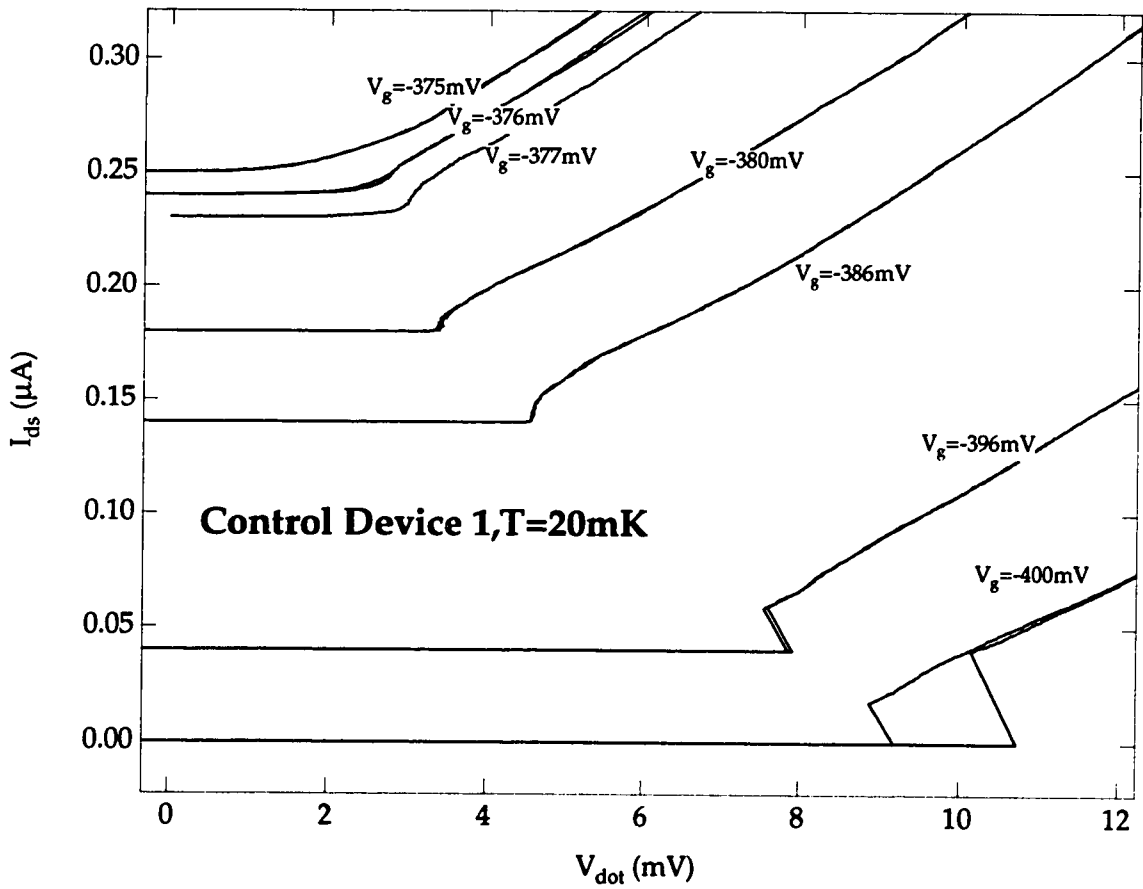
Figure 3.13: The I-V curves of a single dot as a function of the gate voltage.

than this pinch-off value, a single hysteresis loop appears accompanied by upward and downward switching events Fig. 3.13. Here we again define pinch-off as the regime where the device has negligible conductance near zero bias, i.e. the I-V curve has zero slope at the origin.

The I-V curve for the single dot shown in Fig. 3.14 has a very weak temperature dependence compared to that of the array, and the width and location of the hysteresis are unchanged up to $700mK$. As in the array, no hysteresis is seen at $4.2K$ for any gate voltage. Unlike the arrays, no sub-loops or multiple switching events are observed in the single dot. Although the lithographic dimensions of the single dot and array are nominally identical, in all cases, pinch-off of the single dot occurs at a considerably larger gate voltage than for the array. With the available data it is not possible to state clearly whether this difference is due to the details of the device design and fabrication, or whether it results from a significant dot-dot interaction.
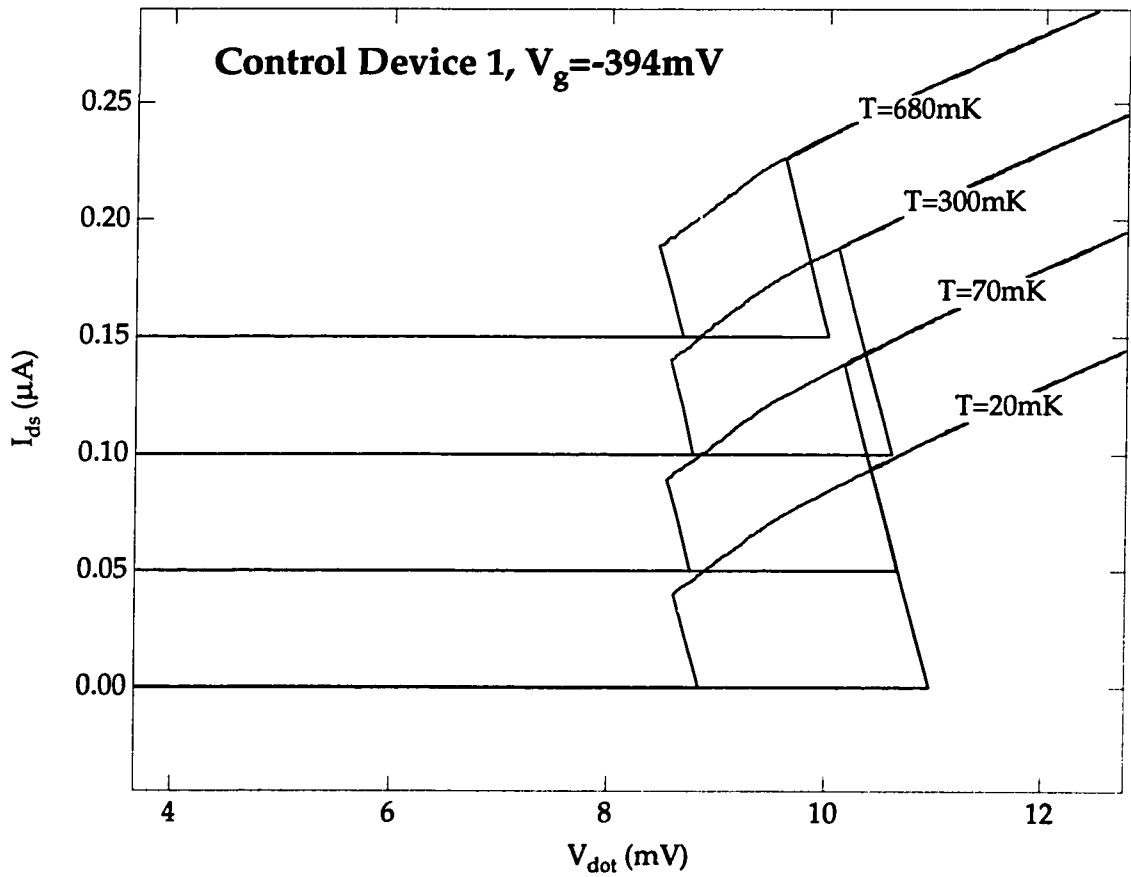
Figure 3.14: The temperature dependence of the I-V curve of a single dot.

Chapter 4

Conduction Threshold:
Non-Hysteretic Regime

4.1 Introduction

In this chapter, the non-hysteretic regime will be discussed. This is the regime in which the array is pinched-off at $V_{arr} = 0$, but there is no significant hysteresis. To study this regime in the arrays, *Device 1* was chosen since its I-V curve did not have a large number of hysteresis loops. It was easier to enter the non-hysteretic regime in the control device since the hysteresis never appears at very low bias voltages.

The most important difference in the curvatures of the I-V characteristics of the arrays versus single dots is the fact that the I-V curves for the arrays are concave upward above a threshold, while for the single dots they are concave downward above a threshold. More quantitatively, both the array and single dot I-V curves can be fit very well with a power law[1] dependence

$$I_{ds} = constant \times (V - V_T)^\varsigma, \qquad (4.1)$$

where V_T is a threshold voltage. This power law and the exponents will be discussed in the next two sections and in Sec. 5.6.

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[1] For the single dot it can be very well fit with $I_{ds} = constant \times (V^2 - V_T^2)^\varsigma$. For $|V - V_T| \ll |V_T|$, this equation reduces to Eqn. 4.1.

Gate Voltage, $V_g(mV)$	Threshold Voltage, $V_T(mV)$	Exponent, ζ
-146	0	1.75
-148	3.65	1.47
-150	5.04	1.42
-152	4.35	1.60
-154	5.56	1.56
-158	10.08	1.43
-162	14.98	1.1

Table 4.1: The threshold voltages and exponents obtained from the power law fits at various gate voltages.

4.2   Conduction Threshold in the Array

The 200 × 200 array in *Device 1* is in the non-hysteretic regime for gate voltages $3 - 10mV$ more negative than the pinch-off voltage. In this region, ζ for the array is in the range $1.4 - 1.7$ (Fig. 4.1 a)). The threshold voltage increases as the gate voltage is made more negative as presented in Table 4.1. Even when hysteresis is present, (at slightly more negative gate voltages) the overall array I-V curve remains concave upward, with a similar power law dependence, with small hysteresis loops and switching events superimposed (Fig. 4.1 b)). For even more negative gate voltages, hysteresis becomes well developed and the exponent ζ decreases towards 1.

Theoretically, an I-V dependence with an exponent 5/3 has been predicted for 2-D quantum dot arrays by Middleton and Wingreen [72] for small capacitive coupling between the dots, which is the non-hysteretic regime in their model. The results presented here are consistent with this prediction. These authors also found an increase in the threshold voltage with smaller capacitive coupling between the dots. Experimentally, as the gate voltage is made more negative, the capacitive coupling between the dots decreases and the threshold voltage increases, also consistent with their results.

With increasing temperature, the threshold voltage decreases as seen in **Fig. 3.7**. Also, at sufficiently high temperatures, the conductance around zero bias (Differential
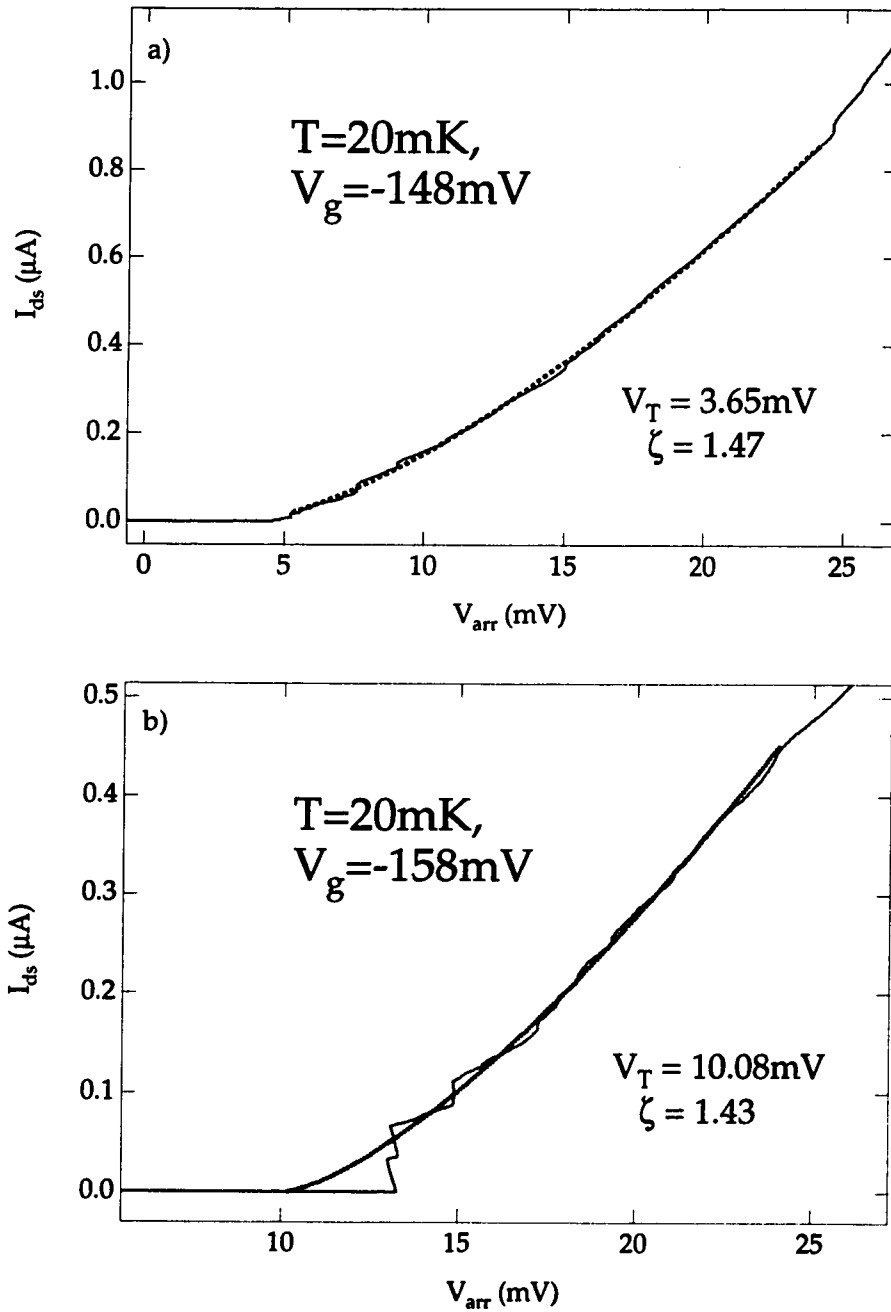
Figure 4.1: The power law fit to the I-V curve of *Device 1* for a) $V_g = -148mV$ and b) $V_g = -158mV$.
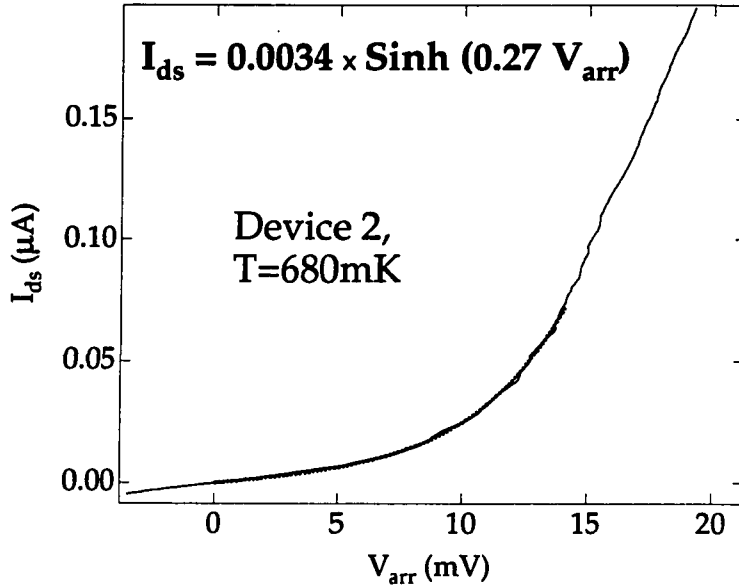
Figure 4.2: The fit to the I-V curve of *Device 2* at $680mK$ around $V_{arr} = 0$.

conductance G) becomes finite. For *Device 2* at $V_g = -115mV$ in Fig. 3.7, this small but finite differential conductance appears above $300mK$. Between $300mK$ and $600mK$, G which is activated, continues to be accompanied by a rapid (super exponential) increase of current around $V_{arr} = 12mV$. However, above $600mK$, this sharp turn-on is washed out and the activated form describes the I-V curve over the full range $|V_{arr}| < 15mV$ (Fig. 4.2):

$$I_{ds} \sim \sinh(constant \times T). \tag{4.2}$$

A similar metal-insulator transition behavior has been recently observed by Lütjering et al. [60].

4.3 Conduction Threshold in the Single Dot

For the single dot, the power law,

$$I_{ds} = constant \times (V_{dot}^2 - V_T^2)^\varsigma, \tag{4.3}$$
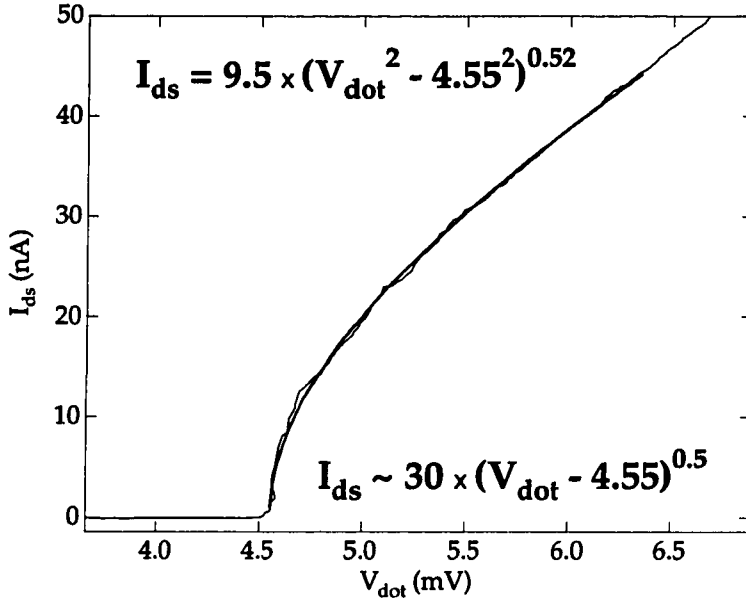
Figure 4.3: The power law fit to the I-V curve of the single dot.

is observed in the range of gate voltages between pinch-off and the hysteretic regime
(Fig. 4.3). For voltages close to the threshold voltage, that is $|V_{dot} - V_T| \ll |V_T|$, Eqn.
4.3 reduces to the same exact power law as in the array,

$$I_{ds} = constant \times (V_{dot} - V_T)^{\varsigma} \tag{4.4}$$

with $\varsigma = 0.5$. For gate voltages corresponding to the non-hysteretic regime, the
array and single dot threshold voltages, V_T are of the same order of magnitude.
Because of the inherent disorder in the array and the exponential dependence of the
tunneling current on barrier height and shape, a large fraction of the applied voltage
will be dropped across a single or few dots, which constitute bottlenecks to the flow
of current. Therefore, the threshold voltage per dot in the array may be comparable
to that of the single dot when one considers only those dots with significant voltage
drops rather than all dots across the array. For the single dot $\varsigma \sim 0.5$ (Fig. 4.3) near
threshold and the I-V curve becomes concave upward only at high bias voltages. The
concave downward shape near threshold ($\varsigma \sim 0.5$) is not found at higher temperatures
($T \sim 4.2K$), and at the same time the possibility for hysteresis at any V_g is also

eliminated.

There is an intriguing similarity between these experimentally observed exponents for the single dot ($\zeta \sim 0.5$) and the array ($\zeta \sim 1.5$), and those in the sinusoidal washboard potential model used to explain the I-V characteristics of pinned Charge Density Waves (CDW's) [35]. For a single degree of freedom, the CDW model gives $\zeta = 1/2$ [35], while the mean field model with many degrees of freedom gives $\zeta = 3/2$ [35] (See also Sec. 5.5).

Chapter 5

Possible Mechanisms for Hysteresis

5.1   Introduction

A very interesting and surprising aspect of the experimental results is the hysteresis observed in the I-V curves of the arrays and control devices. In particular, the hysteresis in control devices requires special attention since the understanding of its mechanism will lead to understanding the hysteresis in the arrays. In this chapter, the gate current measurements will first be described. The gate current in these etched devices is large compared to that in conventional top gated devices. A simple argument which explains this high leakage current will be presented in 5.2.1. Then, a three lead split gate dot which models a single etched dot with gate leakage will be described.

In the next section, electron heating will be considered as another possible mechanism for hysteresis. The results of several recent theoretical studies [47, 59, 32] and their possible connection with the experimental results presented in this dissertation, will be discussed.

It has recently been shown that, similar bistabilities can be connected with impurities and imperfections, in particular DX centers in $AlGaAs$ [11]. These effects will be considered in 5.4.

The results of the transport measurements in the arrays are qualitatively very similar to those seen in strongly interacting systems, such as Wigner solids and charge

density waves. In the last section of this chapter, these systems will be reviewed, and their similarities to the quantum dot arrays will be discussed.

5.2 Gate Current Measurements

All the results discussed in this dissertation up to this section were obtained from devices which were etched about $1000\AA$ deep. However, the I-V curves of other devices which were etched only $300\AA$ did not show hysteresis at all at $20mK$. Each of these devices will be referred to as a *Shallow Device*. The SEM photos of two Shallow Devices are shown in Fig. 5.1 a) and b). Their MBE growth files are given in B.2. The only difference between shallow and deep etched devices is the *Si* doping level and the etching depth. The fabrication process is exactly the same, except the *Shallow Device* being etched only about $300\AA$ deep. They were grown in the same MBE run. The fact that the I-V curves of these devices did not show hysteresis resulted in the conclusion that the mechanism for the hysteresis may be related to the etching depth, and/or the gate current.

5.2.1 Experimental Results

This section summarizes the experimental results of the gate current measurements which are made using hysteretic deep etched devices (*Device 1, 2, 3*) and non-hysteretic shallow etched devices (*Shallow Device*). The gate voltage referenced to the ground was applied to one of the ohmic contacts (e.g. "3" in Fig. 2.8). The potential on gate contact was fixed by connecting it to a current sensitive preamplifier (virtual ground). The gate conductance (dI_g/dV_g) was obtained from the ratio of the small *ac* voltage added to the *dc* voltage source and the *ac* current measured by a lock-in amplifier. The setup for this measurement is shown in Fig. A.1.

Fig. 5.2 shows a) the gate current I_g and b) dI_g/dV_g versus the gate voltage, V_g, for *Device 1* and a shallow etched device at $4.2K$. There is no hysteresis in the curve. This is not surprising since at this temperature, and at $V_{arr} = 0$, the I_{ds} versus V_{arr} does not have hysteresis either and the current is conserved. However, two important
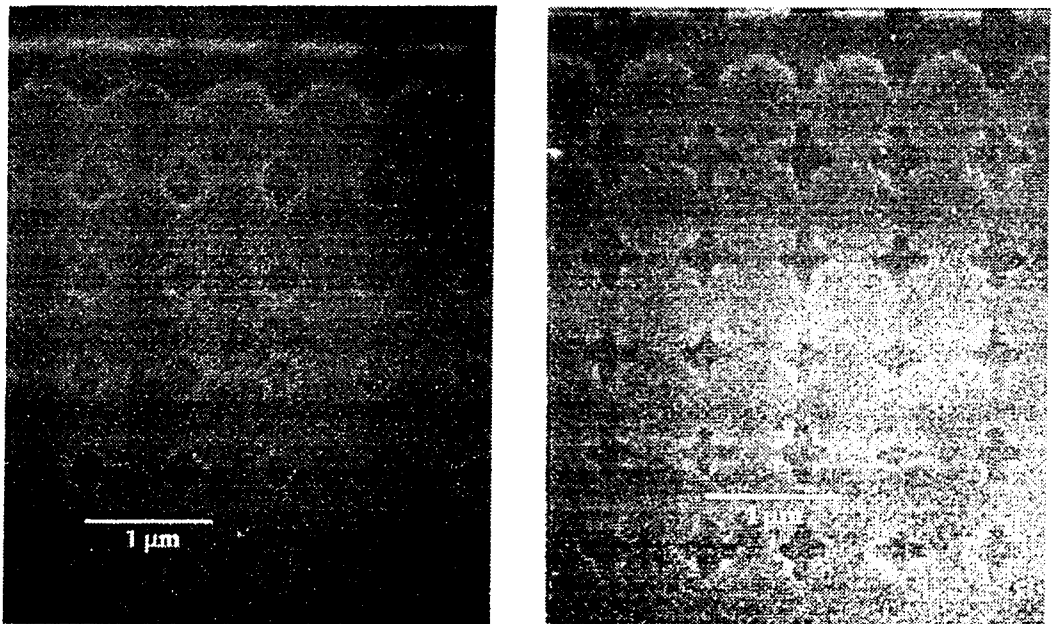
Figure 5.1: SEM photos of shallow etched devices with a) $d = 300nm$ and b) $d = 450nm$.
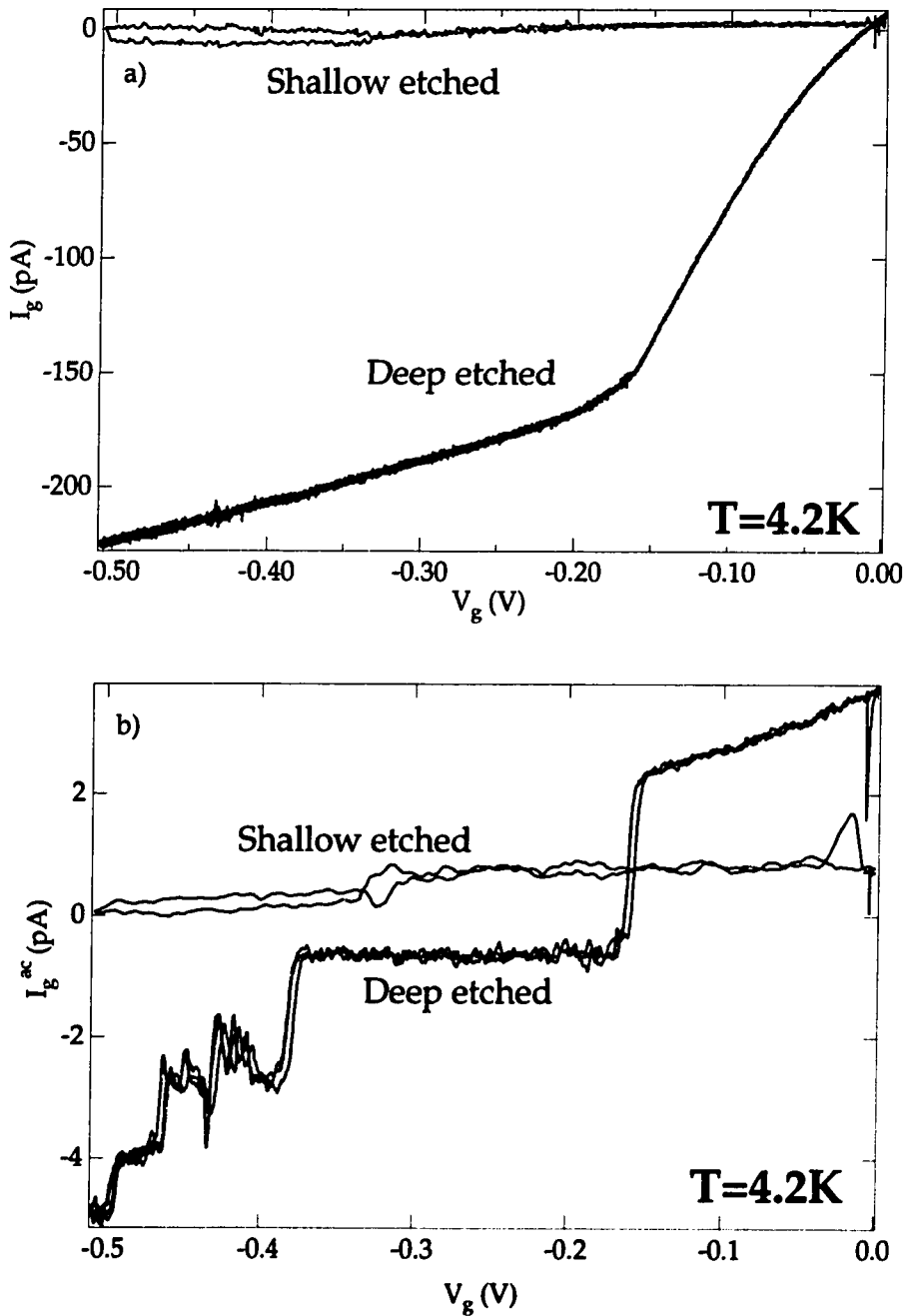
Figure 5.2: a) The gate current and b) its derivative for a deep and a shallow etched device.

aspects of the curves should be noted:

- The gate current in the shallow etched device is about two orders of magnitude lower than that in the deep etched *Device 1*.

- The gate current in *Device 1* has a kink (discrete curvature change) at about $-0.175mV$[1] which is the pinch-off voltage of the array at $4.2K$. This means that the gate current which leaks from one of the sides of the array to the ohmic contact on the opposite side is blocked when the array is pinched off. For more negative gate voltages, the current follows only the paths reaching the ohmic contact directly hence the curve has a smaller slope (or the gate conductance is smaller). This is consistent with the design and layout of the array, control devices and contacts (Fig. 2.2).

When the temperature decreases, a hysteresis loop appears in I_g. Fig. 5.3 a) and b) show the data from the simultaneous measurements of the gate current I_g and the source drain current I_{ds} as a function of V_{arr}[2], at $20mK$.

The measurement setup for this data is shown in Fig. A.2. Both curves show hysteresis at the same threshold voltage, as expected from current conservation.

The gate current measurements show that the etching depth has a significant effect on the gate current. A tunnel barrier is formed between the gate which fills in the etched regions, and the *GaAs* 2-DEG layer shown in Fig. 2.2. The transparency of this barrier is high if the etching depth is larger than the 2-DEG depth. The dependence of the gate transparency on the gate voltage for deep etched devices can simply be calculated using Poisson's equation for the potential in the depletion region show in Fig. 5.4.

Taking $\phi_B = 0.7eV$(mid-gap value for *GaAs*) as the boundary condition, the potential can be calculated as

$$U(x) = \frac{e^2 N_D^*(d-x)^2}{2\epsilon}, \qquad 0 < x < d, \qquad (5.1)$$

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[1] This can be noticed clearly from the simultaneous *ac* lock-in measurement result in Fig. 5.2.

[2] V_{arr} was chosen as the independent variable to be consistent with the data obtained before.
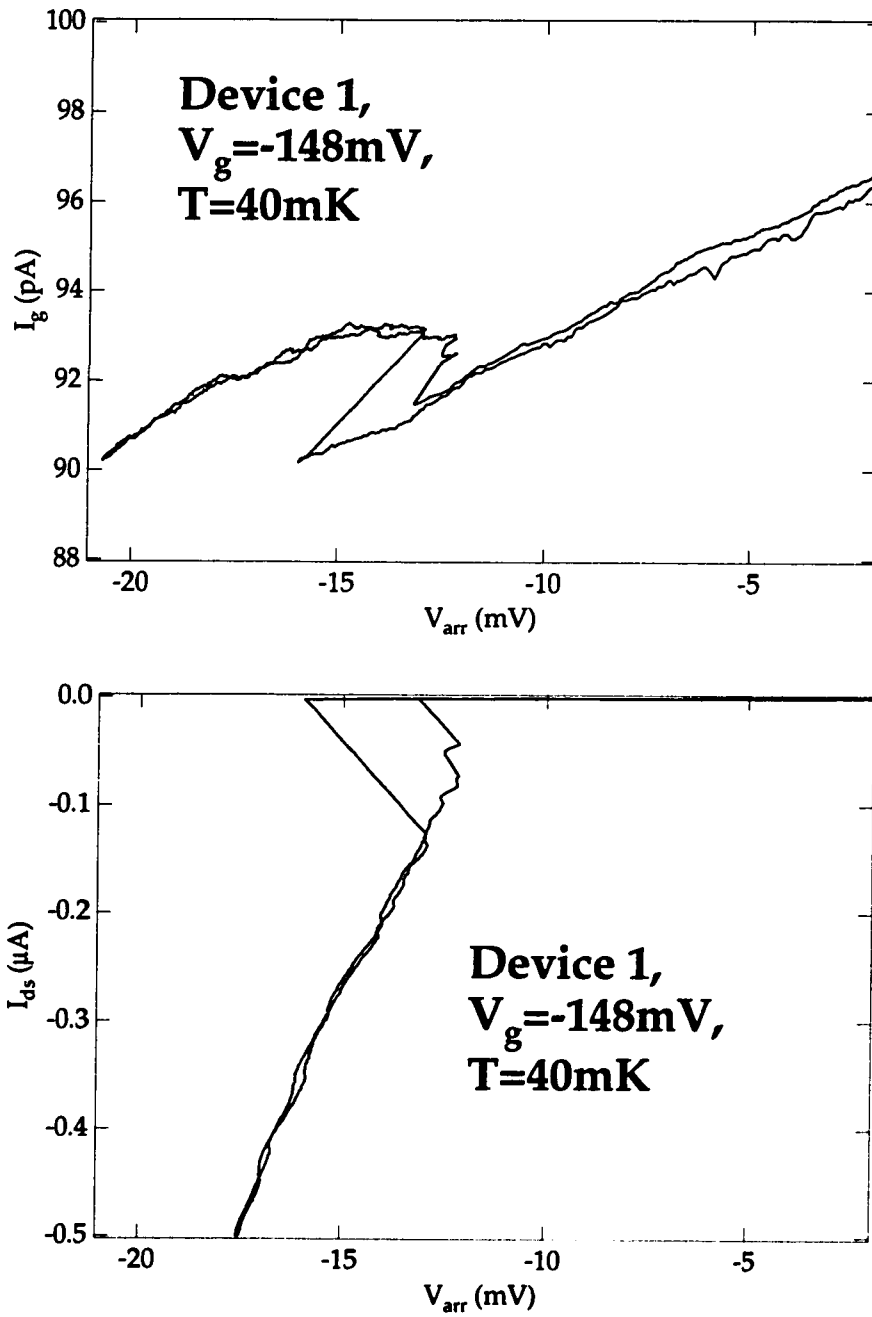
Figure 5.3: The gate current versus V_{arr}.
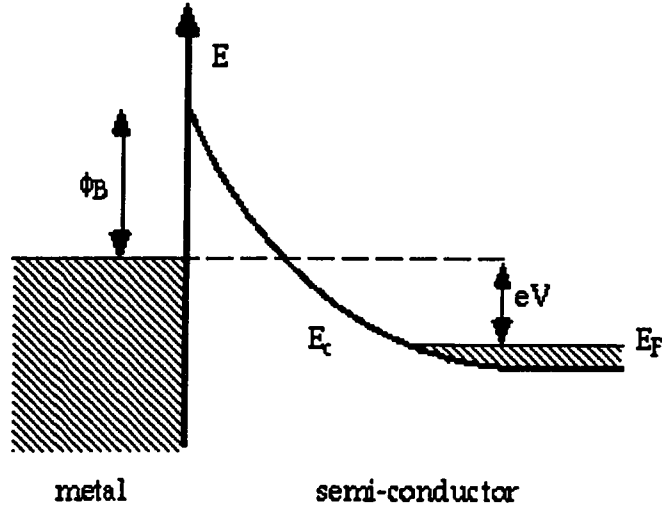
Figure 5.4: A tunnell barrier formed between the dot and the gate.

and the depetion length as

$$d = \left[\frac{2\epsilon(\phi_B + V_g)}{eN_D^*} \right]^{1/2}.$$

(5.2)

Here, $U(x)$ is measured from the Fermi energy of *GaAs*, and the coordinate x is measured from the interface into *GaAs*. In this structure, the ionozed donors and the plane of the 2-DEG are spatially separated because of the spacer. Therefore the depletion region is wider than what it would be if the ionized donors were near the 2-DEG. In the above equations, their fringing field which causes this large depletion length is taken into account by using an effective donor concentration, N_D^*, which can be found using Eqn. 5.2 and assuming $d \sim 1000\overset{\circ}{A}$ for $V_g = 0$ (from experiments). To get an idea about the transparency, the thickness of the barrier at the gate Fermi level, d_0, should be considered. Setting the left hand side of Eqn. 5.1 to V_g, one can find

$$d_0 = d - \sqrt{\frac{2\epsilon V_g}{N_D^* e^2}},$$

(5.3)

and therefore,

$$d_0 = \sqrt{\frac{2\epsilon}{N_D e^2}} \left(\sqrt{V_g - \phi_B} - \sqrt{V_g} \right). \tag{5.4}$$

It is easy to see that d_0 is a monotonically decreasing function of V_g. Since the transparency of the gate barrier, Γ_g, increases with decreasing thickness at the Fermi energy, the gate current increases as $|V_g|$ is increased. The dot-to-dot transparency, Γ_d, however, decreases as the gate voltage is made more negative. If $V_g = 0$,

$$\Gamma_g \ll \Gamma_d.$$

If $|V_g| \gg |V_p|$, where V_p is the pinch-off voltage,

$$\Gamma_g \gg \Gamma_d.$$

This means that there must be a gate voltage such that

$$\Gamma_g \sim \Gamma_d.$$

The change of transparencies as a function of the gate voltage is schematically shown in Fig. 5.5.

5.2.2 Three Lead Single Dot

The etched single dot can be thought of as a three terminal device with the gate being the third terminal. However, in etched devices, as shown in the previous section, Γ_g and Γ_d cannot be adjusted independently from each other. This makes it very hard to prove that the hysteresis is due to a mechanism involving gate leakage.

These facts lead to the conception of a split gate three lead single dot, in which all the tunnel barriers can be tuned independently. Such a dot was fabricated by electron beam lithography and subsequent gate lift-off. The MBE growth file for the sample is given in B.3. The fabrication procedure is similar to that described in Chapter 2. However, the optical lithography was done first. Then a bilayer PMMA was spun, baked and then exposed at $575 \mu C/cm^2$ with a beam current of $1nA$ in a JEOL e-beam machine. Gates were evaporeted in an e-beam evaporator. The layer thicknesses were Ti/Au, $300\text{Å}/1000\text{Å}$. After the evaporation, the sample was dipped
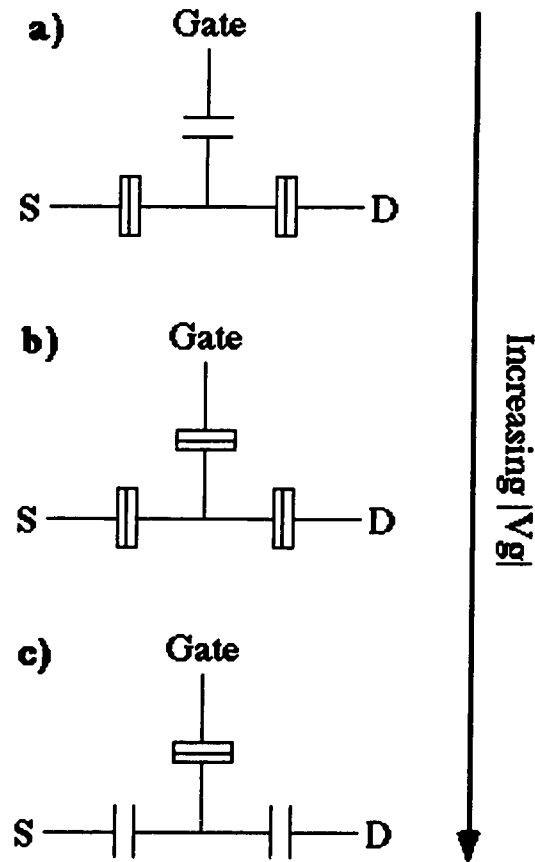
Figure 5.5: The transparencies of the gate and dot barriers. The double parallel lines denote capacitors in which tunneling is negligible. Double rectangles denote tunnel capacitors.

in Acetone to achieve the lift-off. The SEM photo of the device is shown in the inset of Fig. 5.6. The numbers denote the gates and the letters S, D and G refer to *Source*, *Drain* and *Gate* respectively. Here G is the 2-DEG reservoir which is equivalent to the single gate in the arrays. The gate current in the etched devices is simulated by allowing a small leakage from the barrier formed by gates "1" and "4"[3].

Fig. 5.6 shows $400mK$ Coulomb blockade oscillations, obtained by sweeping the voltage V_{g2} on 2 and measuring the *ac* source-drain current using the *ac* lock-in technique. V_{g4} and V_{g1} were set such that there is no leakage from G into the dot[4].

The measurement configuration described in Fig. 2.8 was used to look at the I-V curves. At $400mK$, no hysteresis was observed in the three lead device for the range of parameters corresponding to those of the etched single dot.

5.2.3   Orthodox Theory

Orthodox theory of Coulomb blockade can be used to calculate the I-V curves of a quantum dot in the presence of a third lead.

Similar to Ref. [6], the master equation for the probability, $\sigma(n,t)$, of the charge state with definite number, n, of excess electrons in the central electrode can be written as follows Fig. 5.7:

$$\frac{\partial \sigma}{\partial t} = \sum_{\pm} \sum_{j=1}^{3} \sigma(n \pm 1, t)\Gamma_j^{\mp}(n) - \sigma(n,t) \sum_j \left[\Gamma_j^+(n) + \Gamma_j^-(n) \right]. \tag{5.5}$$

Here $\Gamma_j^{\pm}(n)$ is the tunneling rate through the jth junction ($j = 1, 2, 3$) which leads to an increase $(+)$ or decrease $(-)$ of the charge number n. It depends on the energy gain, $\Delta E_j^{\pm}(n)$, due to tunneling and can be calculated using [3]

$$\Gamma_j^{\pm} = (e^2 R_j)^{-1} \Delta E_j^{\pm}(n) \left\{ 1 - exp[-\Delta E_j^{\pm}(n)/T] \right\}^{-1}. \tag{5.6}$$

In the above equation, R_j denotes the tunneling resistance of junction j and depends on the density of states near the Fermi energy [3]. The energy gains for the junctions

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[3]One of the other barriers could be chosen for gate leakage. It is, however, easier to see conductance oscillations with this particular choice of source and drain, because the potential in the dot is more symmetric for a given V_G.

[4]This is necessary because it is possible to observe Coulomb blockade, if the number of electrons in the dot is a good quantum number.
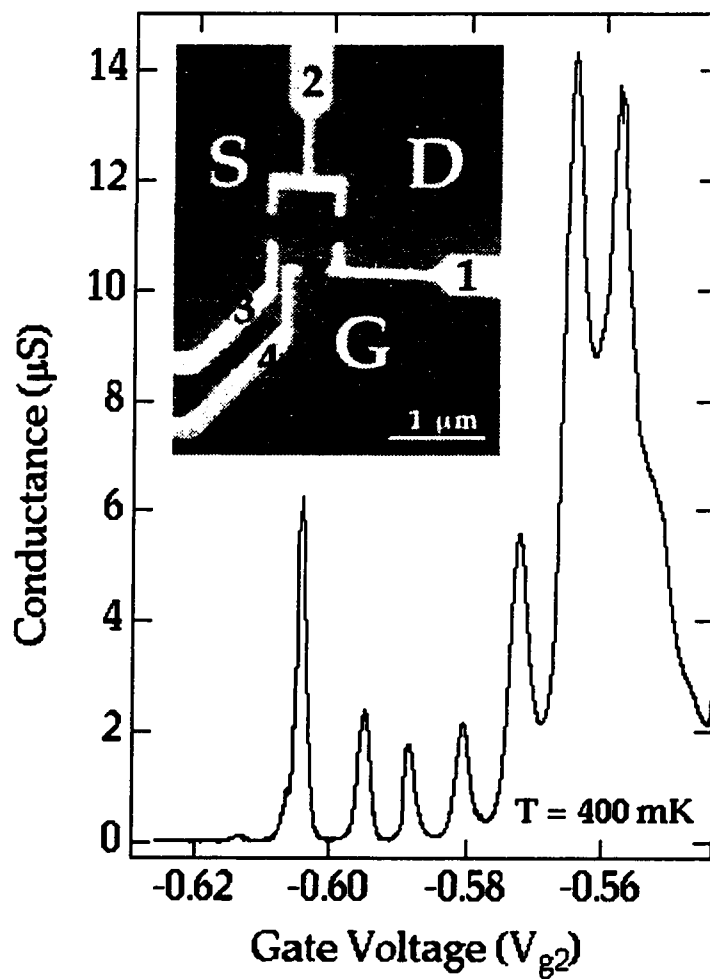
Figure 5.6: The Coulomb blockade oscillations in a three lead dot. The inset shows the SEM picture of the device.
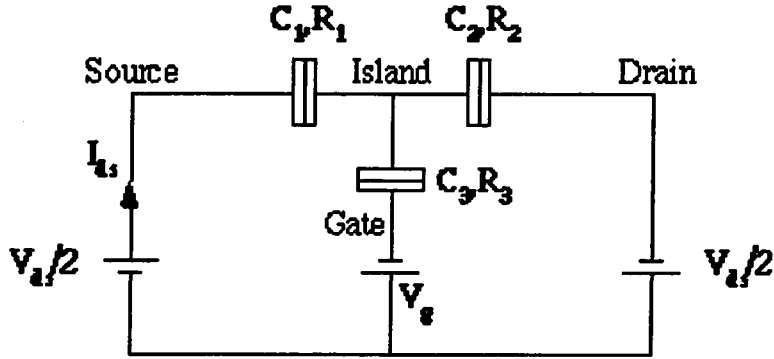
Figure 5.7: The equivalent circuit for the three lead dot.

1, 2, 3 are given by

$$\Delta E_1^{\pm}(n) = \frac{e}{C_\Sigma}\left[-\frac{e}{2} \pm \left(ne + C_g V_g + (C_2 + \frac{C_g}{2})V\right)\right]. \tag{5.7}$$

$$\Delta E_2^{\pm}(n) = \frac{e}{C_\Sigma}\left[-\frac{e}{2} \pm \left(ne + C_g V_g - (C_1 + \frac{C_g}{V_g})V\right)\right] \tag{5.8}$$

$$\Delta E_3^{\pm}(n) = \frac{e}{C_\Sigma}\left[-\frac{e}{2} \pm (ne - (C_1 + C_2)V_g) - (C_2 - C_1)\frac{V}{2}\right] \tag{5.9}$$

respectively. Here, $C_\Sigma = C_1 + C_2 + C_g$. The current, I_j, flowing through the junction j can then be found from

$$I_j = (-1)^{j+1}\sum_{n=0}^{\infty}\left[\Gamma_j^+(n) - \Gamma_j^-(n)\right]\sigma(n), \tag{5.10}$$

where $\sigma(n)$ is the value of $\sigma(n,t)$ as $t \to \infty$, for a fixed n.

Eqn.'s 5.10 and 5.6 form a complete set of equations of the orthodox theory for the three lead dot. They can be solved numerically. The master equation (Eqn. 5.5) can be written as

$$\frac{\partial \sigma(n,t)}{\partial t} = \Gamma^+(n-1)\sigma(n-1,t) + \Gamma^-(n+1)\sigma(n+1,t) - \Gamma(n)\sigma(n,t) \tag{5.11}$$

where

$$\Gamma^{\pm}(n) = \sum_{j=1}^{3} \Gamma_j^{\pm}(n),$$

and

$$\Gamma(n) = \sum_{\pm} \sum_{j=1}^{3} \Gamma_j^{\pm}(n).$$

Eqn. 5.11 is very similar to a diffusion equation except the coefficients are a function of n. There are several numerical approaches to solve these types of equations. The approach to discretizing the time variable is very important in determining the stability of the result. Since only the steady state value of σ is needed, the fastest and most efficient way is to use the "fully implicit"(or "backward time") scheme [78]. In this scheme, Eqn. 5.11 is written as:

$$\sigma(n, t_{j+1}) - \sigma(n, t_j) = \Delta t \times$$
$$\left[\Gamma^{+}(n-1)\sigma(n-1, t_{j+1}) + \Gamma^{-}(n+1)\sigma(n+1, t_{j+1}) - \Gamma(n)\sigma(n, t_{j+1}) \right] \quad (5.12)$$

or

$$\sigma(n, j) = -\Gamma^{+}(n-1)\sigma(n-1, j+1)\Delta t-$$
$$\Gamma^{-}(n+1)\sigma(n+1, j+1)\Delta t + (1 + \Gamma(n)\Delta t)\,\sigma(n, j+1). \quad (5.13)$$

Therefore, at each time step t_j, one has to solve the simultaneous linear equations given by Eqn. 5.13 to obtain $\sigma(n, j)$. This is, on the other hand, a simple problem since the system is tridiagonal. An algorithm is given in Ref. [78]. A convenient choice of initial condition is $\sigma(n, t = 0) = \delta(n)$. The boundary condition for n can simply be taken as $\sigma(n = \pm N_{max}, t) = 0$, with $N_{max} = 100$. The code was written in the software "Igor Pro", and is given in Appendix D.

Fig. 5.8 shows the results of the I-V curve calculation for various gate voltages. The solid line represents the I-V curve in the absence of leakage from the third lead ("gate leakage") and exhibits Coulomb staircase [49] ($V_G = 0$). The dotted and dashed lines are for finite gate voltages and non-zero transparencies. As the gate voltage becomes more negative, the staircase gets washed out and the Coulomb gap disappears. Moreover, none of the curves shows hysteresis: Since there are no actual
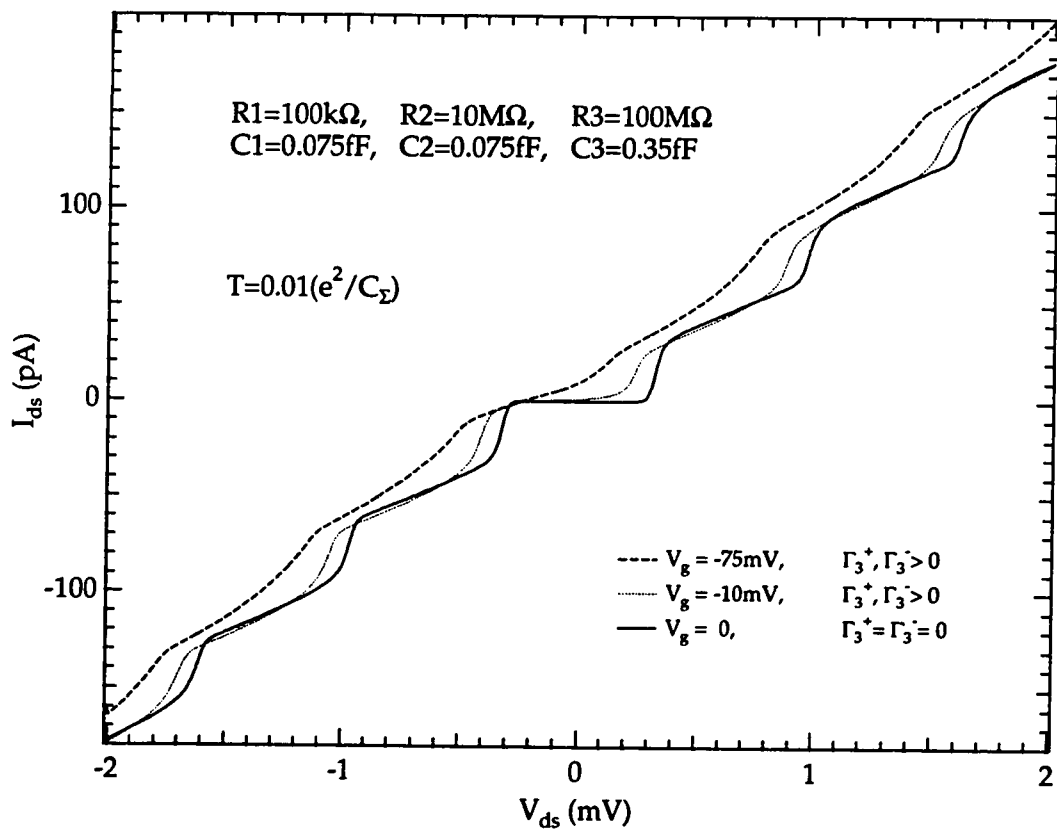
Figure 5.8: The I-V curves of the three lead dot for various gate voltages and transparencies.
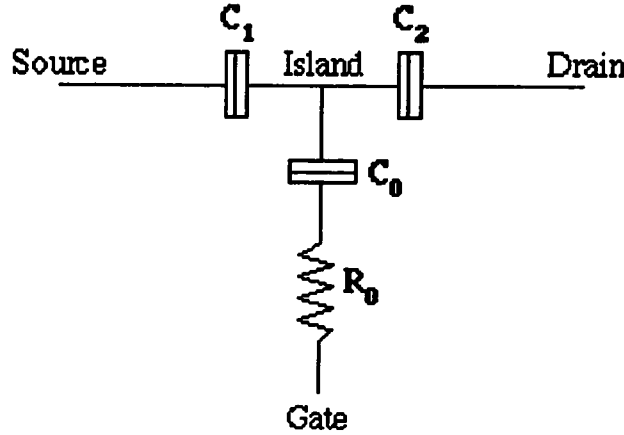
Figure 5.9: The RC-SET model (From Ref. [44]).

resistors in the coupling circuit, no multiple stable charge states are possible in the single dot.

5.2.4   RC-SET Model

The orthodox theory shows that there can be no hysteresis in a single dot if the coupling circuit consists of capacitive elements only. If the control potential (V_g in this case) is applied through a large resistor, however, the charge distribution does not change on each capacitor during or between tunneling events. This means that the device has memory, and the I-V curve can exhibit hysteresis.

Transport through a single dot in which the coupling circuit consists of a large resistor and a capacitor has recently been investigated by Korotkov [44]. If $R_0 \gg R_Q C_\Sigma / C_g$, the coupling circuit does not affect the double junction system (junctions 1 and 2) during the tunneling event. In other words, the capacitance $C_1 + C_2$ which is charged during a tunneling event is different than the total capacitance C_Σ (Fig. 5.9). However, between the tunneling events, the effective charge Q, which is the total charge on C_1 and C_2, may change due to the current through R_0.

In Ref. [44], the author used the orthodox theory to calculate the probability

density, $\sigma(n, Q, t)$, in the limits of small coupling resistance ($R_0 \ll min(R_1, R_2)C_\Sigma/C_0$ but still $R_0 \gg R_Q C_\sigma/C_g$) and large coupling resistance ($R_0 \gg (R_1 + R_2)C_\Sigma/C_0$). The difference of this calculation from the theory presented in the previous section is that the energy gain, $\Delta E_j^\pm$, does not directly depend on n but only on the effective charge, Q. The I-V curve in the large coupling resistance case exhibits multiple switching and hysteresis.

The multistability calculated by the RC-SET model is very similar to experimentally observed switching and hysetresis in the arrays, and single dots [44]. However, in these devices, there is no large resistance in series with the gate voltage. Moreover, the current in the single dot after switching is so large that, $R_j \gg R_Q$ cannot be satisfied. This means that, the mechanism for the hysteresis in the control device is different that that proposed by the RC-SET model. However, the RC-SET model can explain the hysteresis in the arrays: A dot in the array which, in isolation, would not be hysteretic can be pushed into the hysteretic regime by the impedances of its neighbors, which effectively raise R_0, R_1 and R_3 for that dot. In the case of arrays the large current scale after switching can be explained by a parallel current path.

5.3   Electron Heating

Several theoretical models have proposed a hot-electron related bistability to explain the I-V curves of quantum dots [47, 59, 32]. In this section, two of these models will be summarized and their possible connection with the bistable I-V curve of the control devices will be discussed.

5.3.1   Thermionic Emission Model

The first model uses an energy balance approach to describe heating of electrons trapped inside the dot [32] to explain the experimental results of Wu et al. [94]. The authors assume that the dimensions of the dot are sufficiently large that the electrons inside can be treated as a finite extent two dimensional electron gas (2-DEG). Their second assumption is that electrons injected over the input barrier A thermalize
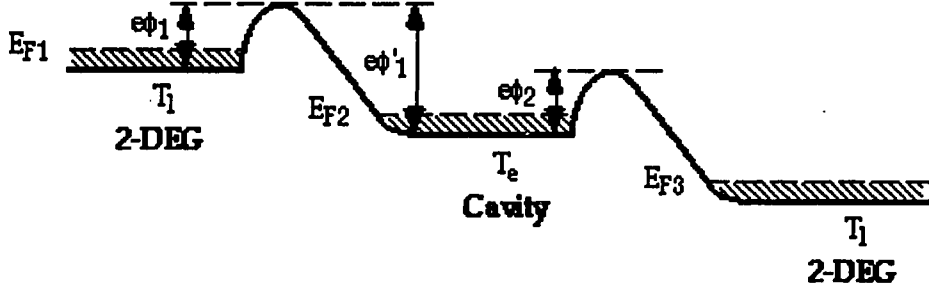
Figure 5.10: Schematic diagram showing two barriers in series (From Ref. [32]).

through electron-electron scattering with the electrons inside the dot, which are then thermionically emitted over the second barrier, B [32] (Fig. 5.10).

Tunneling is also neglected, so that the current is carried only by thermionic emission over the two barriers. The model calculates the barrier heights, ϕ_1 and ϕ_2, and the injection energy, $e\phi_1'$, shown in Fig. 5.10, as a function of the source-drain voltage, V_{sd} and the number of electrons inside the dot, N. The thermionic emission current, I_i, at barrier i $(i = 1, 2)$ is given by:

$$I_i = C_i e^{-e\phi_i/kT_i}, \tag{5.14}$$

or, the barrier heights are given by:

$$\phi_i = \frac{kT_l}{e} \ln \frac{C_i}{I_i}. \tag{5.15}$$

In equations 5.15 and 5.14, C_i are constants which depend on the density of states, the width of the barrier, the mean velocity of electrons incident on the barrier, electron density and the lattice temperature, T_l (For more details see for example Sze [85]). The injection energy, $e\phi_1'$, is related to the current, electron temperature, T_e, and the number of electrons, N, through the energy balance equation:

$$I \times \left(\phi_1' + \frac{kT_l}{e} - \phi_2 - \frac{kT_e}{e} \right) = N \left\langle \frac{\partial E}{\partial t} \right\rangle_{coll} \tag{5.16}$$

Here, the term on the right hand side represents the energy loss rate for N electrons, and is related to the typical times of the phonon emission processes.

Once the current $I = I_1 = I_2$ is chosen, ϕ_i, ϕ_1', N, V_{sd}, T_e can all be found self consistently. One finds that, as the current goes up, the electron temperature goes up and the electron number goes down. This means that the high current state has fewer electrons, than the low current state, and the electron temperature in the high current state is higher than that at low current state.

To compare the above theoretical results with the experimental single dot results in Chapter 3, it is necessary to estimate the number of electrons in the Control Device. For $V_g = 0$, assuming a sheet electron density $n_s = 3 \times 10^{11} cm^{-2}$, and a circular dot with a radius, $r = 100nm$, the number of electrons can be found to be

$$N = n_s \pi r^2 \simeq 100 \qquad (5.17)$$

Since the devices are top gated, the density decreases as the gate voltage is made more negative. This decrease is relatively slow for V_g down to -100, but for V_g less than $-200mV$ the decrease becomes very sharp [90]. For the arrays, the density can be assumed to be constant, since the lowest pinch-off voltage is about $-150mV$. The typical pinch-off voltages for deep etched single dots, however, are on the order of $-400mV$. Therefore, at the gate voltages around which the hysteresis is observed, the electron number is about one order of magnitude smaller than that in the devices measured by Wu et al. [94]. Moreover, the typical current after switching in deep etched devices ($\simeq 0.1\mu A$), is also an order of magnitude smaller. These estimates are consistent with the fact that, the bistability in the etched devices disappears at $4.2K$, whereas, the bistability in the devices of Wu et al. persists up to temperatures much higher than $4.2K$.

Although the model of Goodnick et al. gives the correct order of magnitude estimates for the hysteresis in the deep etched devices, it does not explain why shallow etched devices which have very similar dimensions and electron densities don't show bistability.

5.3.2 Heating in the Coulomb Blockade Regime

Several theoretical models to treat the electron heating in the Coulomb blockade regime have recetly been proposed by Liu et al. [59] and by Korotkov et al. [47]. Since the former does not give bistability in the I-V curve, it will not be considered here. The model by Korotkov et al. [47] is a self-consistent calculation of the electron temperature of the central electrode (dot), T_m, for given outer electrode temperatures, T_j, where $j = 1, 2$. The authors assume that the device is in the Coulomb blockade regime (i.e., the electrons tunnel between the electrodes), and the parts of the middle electrode adjacent to each junction, j, have temperatures equal to T_j. They use the orthodox theory with temperature dependent tunneling rates,

$$\Gamma_j^{\pm}(n) = \Gamma \left[\Delta E_j^{\pm}(n), T_j, T_m \right].$$

The typical hysteresis width and the typical current can be estimated as $0.5mV$ and $20pA$ respectively [47].

The above estimated current value is about two orders of magnitude smaller than those measured in the etched single dots in this dissertation. Therefore, it is unlikely that, electron heating in the Coulomb blockade regime is the cause of the hysteresis in etched single dots. However, switching currents as low as $400pA$ (see Fig. 3.4) have been measured in the arrays. Hence, the model proposed by Korotkov et al. can explain some of the hysteresis loops observed in the array I-V curves.

5.4 Defects and Impurities

It is well known that, defects and impurities that have two metastable states can cause telegraph noise and related hysteresis in the electrical characteristics of devices. In this section, DX centers, surface impurities, and their possible connection with the experimental results will be discussed .

5.4.1   *DX* Centers

The defect which gives rise to a deep donor level in $Al_xGa_{1-x}As$ alloys for $x \geq 0.22$ is commonly known as the *DX* center [54, 13]. In the nondegenerate limit, the *DX* center is proposed to result from the following set of reactions [14]:

$$d^0 \rightarrow d^+ + e$$
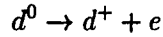
which involves the emission of an electron and,

$$d^0 + e \rightarrow DX^-$$
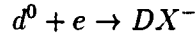
which involves the capture of a free electron. The two equations add up to give

$$2d^0 \rightarrow d^+ + DX^-.$$
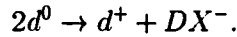
In the equations above, d represents a fourfold coordinated substitutional donor (like *Si* in *AlGaAs*); *DX* and e denote the broken-bond configuration shown in Fig. 5.11 and a free electron in the conduction band respectively. The superscripts specify the charge states.

The configuration coordinate diagram for the *DX* center is shown in Fig. 5.12 [75]. In this diagram, the parabolas on the left hand side represent the total energy when the electron is in the conduction band (i.e. *DX* center ionized), and the one on the right hand side represents the total energy of the occupied *DX* center. The shift along the horizontal axis represents a change in the atomic configuration around the *Si* atom when the charge state is changed. The *DX* center is characterized by four energies (the numerical values are for *Si* in *AlGaAs*):

- $E_d \simeq 0.175 - 0.205eV$, the donor binding energy with respect to the bottom of the conduction band.

- $E_e \simeq 0.43eV$, the activation energy for the emission of an electron from the *DX* level to the conduction band.

- $E_b \simeq 0.21eV$, the capture energy measured with respect to the *L* minimum of the conduction band.
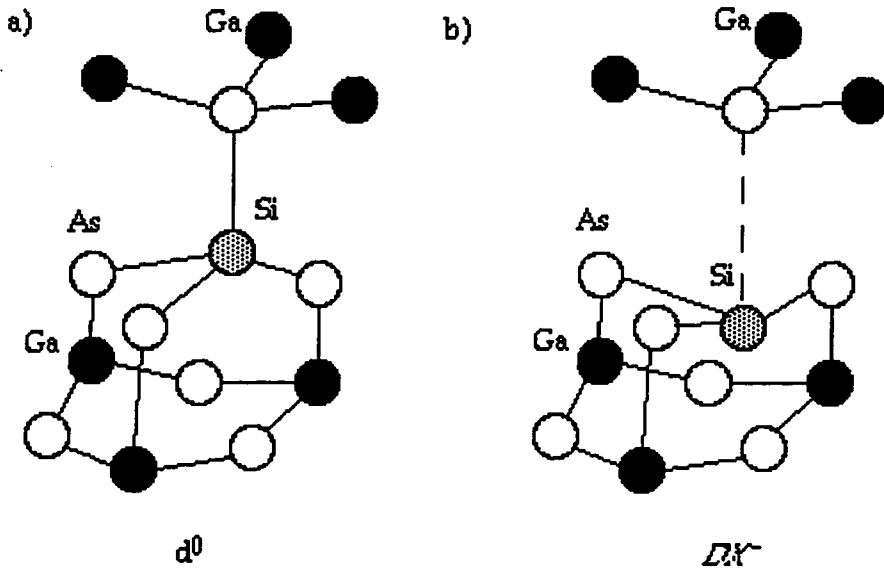
Figure 5.11: The schematic diagram which depicts the arrangement of atoms commonly called a DX center (From Ref. [14]).
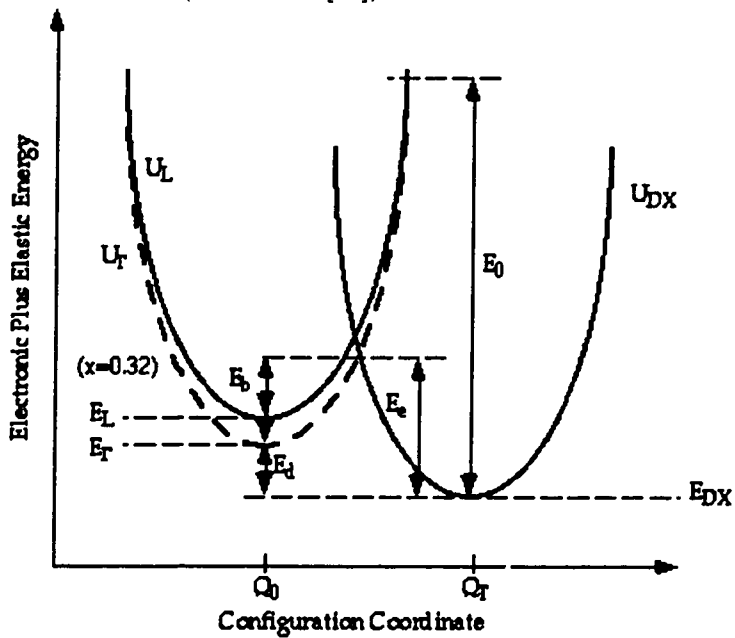
Figure 5.12: Configuration coordinate diagram for the DX center (From Ref. [75]).

- $E_c \simeq 0.22eV$, the activation energy for the capture of an electron from the conduction band measured with respect to the bottom of the conduction band ($E_c = E_e - E_b$).

In the diagram, E_L, E_Γ and E_0 represent the minimum of the L valley, the minimum of the Γ valley and the optical ionization energy respectively ($E_0 \simeq 1.25 - 1.45eV$).

DX centers have several known effects on heterojunction device characteristics, in particular that of modulation doped 2-DEG structures. Two of them are:

- Persistent photoconductivity which results from the ionization of the DX center at low temperatures. When the sample is exposed to light, with energy larger than E_0, the DX center is ionized. When the light is turned off, however, the electrons remain in the conduction band, and depending on the alloy composition and temperature, this photoconductivity may decay in minutes to days [12].

- Hot electron trapping. Once the source drain voltage exceeds some critical value (about $1.0V$ in a device with $1\mu m$ gate length), the DX center captures the hot electrons, and the device resistance increases. The normal characteristics can be recovered if the temperature is increased to about $150K$ or if the device is exposed to light.

The possible connection between the bistability in the array I-V curves and the DX centers can be investigated by considering a recent experiment on $GaAs/AlGaAs$ split gate quantum waveguide structures [11], fabricated by lift-off. In this experiment the I-V curve exhibits random telegraph noise, switching and hysteresis, induced by illumination. The bistability can be eliminated by annealing the sample at about $120K$ for $12h$. This annealing temperature and the corresponding time scale are consistent with the results of Mooney et al. [75], which provides strong evidence for the important role DX centers play in low temperature transport in $GaAs/AlGaAs$ mesoscopic systems.

The quantum dot arrays and control devices in this thesis, on the other hand, did not exhibit any random telegraph noise, within the investigated parameter space.

Moreover, the hysteresis was present without illumination. The source drain voltage was swept relatively slowly ($\sim 0.05mV/sec$ in some cases) and the curves were extremely robust at $20mK$, even after a waiting period of two weeks Fig. 5.13. The stable nature of the curves did not change up to $700mK$. These facts lead to the conclusion that the time constants for the arrays and control devices are very large at the temperatures the data in this dissertation was taken.

It is not currently possible to relate the mechanism for the hysteresis in the arrays and control devices to the occupancy of DX centers: First, the electrons in the 2-DEG cannot tunnel into the doped $AlGaAs$ layer and change the occupancy, because of the thick spacer. Second, the activation energy, E_e for the emission to the conduction band is very large, so DX centers cannot be formed or destroyed at the measurement temperatures. In the experiment of Berven et al. [11], the sensitivity of the I-V curves on the DX center configuration is likely to be due to a change in the potential profile. In other words the bistability is related to a mechanism which involves the potential profile, but not the DX centers directly.

5.4.2   Impurities

Except for the results reported in Ref.'s [94, 11], multi-stabilty has only been observed in the I-V curves of etched devices. This suggests the possibility of surface and interface states being the source of the hysteresis in the case of top gated arrays and control devices. A simple model describes how an impurity site can become charged by an electron as current flows. Once trapped, the electron can tunnel to the site which is located at the $GaAs/CrAu$ interface or the $GaAs$ surface in the experiment of Pilling et al. (See Sec. 1.4.3). This extra electron then changes the potential profile on the current path of the electrons and cause hysteresis.

The effect of impurities on the potential profile can be seen more clearly at gate voltages close to the unprocessed 2-DEG pinch-off value, which is $-630mV$ for the samples in B.1 and B.2. Some of the single barrier control devices which pinched-off at less than $-450mV$, had single hysteresis loops very similar to those of single dot control devices. The hysteresis and switching in this case is likely to have resulted
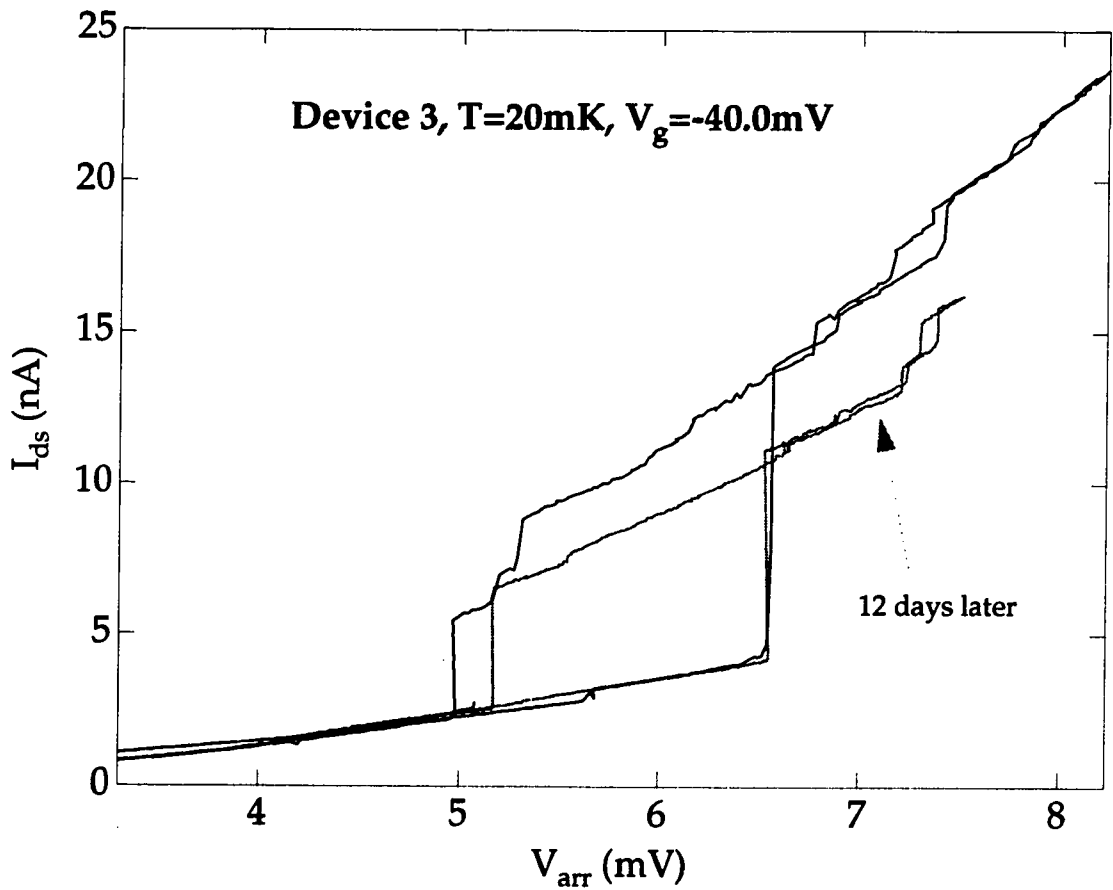
Figure 5.13: Two I-V curve traces, obtained twelve days apart from each other within the same cooldown.

from the formation of "accidental dots" by impurities and etching.

5.5   Strongly Interacting Systems

5.5.1   Charge Density Waves

Charge Density Waves (CDWs) were first discussed by Frölich in 1954 and by Peierls in 1955. They are broken symmetry states of metals, brought about by electron-phonon or electron-electron interactions. The charge density is not uniform, but exhibits a periodic spatial variation.

The dynamics of the collective mode due to electron-phonon interaction can be described in terms of a position and time dependent complex order parameter

$$\Delta(x,t) = \Delta e^{i\phi}, \tag{5.18}$$

such that

$$\rho(x) = \rho_0 + \frac{\Delta \rho_0}{\lambda' v_F k_F} \cos(2k_F + \phi). \tag{5.19}$$

Here ρ_0, λ', v_F and k_F represent the electron density in the absence of interaction, the dimensionless electron phonon coupling constant, the Fermi velocity and the Fermi wave vector, respectively [35]. At low temperatures, the amplitude fluctuations in the order parameter do not play an important role and by treating the phase as a classical field, the Lagrangian density in one dimension can be written as [26]:

$$\mathcal{L} = \frac{n_c}{4\pi} \left[\frac{m^*}{m v_F} \left[\frac{\partial \phi}{\partial t} \right]^2 - \kappa^2 \left[\frac{\partial \phi}{\partial x} \right]^2 \right] \tag{5.20}$$

where n_c and m^* are the density of condensed electrons along the chain direction and effective mass of the condensate, respectively. The first term on the rigth hand side represents the kinetic energy of a line mass, $m^* n_c$, per unit length. The second term corresponds to the potential energy associated with the distortion of the collective mode, with a phenomenological elastic constant κ. The equation of motion for this Lagrangian is then

$$\frac{\partial^2 \phi}{\partial t^2} = \frac{m}{m^*} \kappa^2 \frac{\partial^2 \phi}{\partial x^2} \tag{5.21}$$

The solutions of Eqn. 5.21 are of the form, $exp\,[i(wt - qx)]$ (plane waves), and the $q = 0$ mode corresponds to the translational motion of condensed electrons with the ions oscillationg around their equilibrium positions. The rigid displacement of the CDW leads to a current density given by:

$$j_{CDW} = \frac{e}{\pi}\frac{\partial\phi}{\partial t}.$$ (5.22)

The compression of the wave leads to a change in the density, and therefore

$$n_c = \frac{e}{\pi}\frac{\partial\phi}{\partial x}$$ (5.23)

The equations 5.22 and 5.23 lead to the continuity equation given by:

$$\frac{\partial j_{CDW}}{\partial x} + \frac{\partial n_c}{\partial t} = 0$$ (5.24)

In the above analysis, inhomogeneities are neglected. In most experimental situations, however, there are impurities and defects which lead to the formation of pinning centers with a finite pinning energy (and the corresponding pinning frequency, ω_0). This results in a finite dc threshold for nonlinear conduction. An equation of motion for the phase in the presence of an electric field and a single pinning center was proposed by Grüner et al.[36]. In this so called "single-particle" in a "washboard potential" model shown in Fig. 5.14,

$$\frac{1}{\tau}\frac{\partial\phi}{\partial t} + \omega_0^2\sin\phi = \frac{2k_FeE}{m^*}.$$ (5.25)

In the presence of a constant electric field, the average current is obtained by solving 5.25, and is given by

$$\langle J(t)\rangle = \begin{cases} \sigma_N E + (n_{CDW}e^2\tau/m^*)(E^2 - E_T^2)^{1/2} &, \quad E > E_T \\ \sigma_N E &, \quad E < E_T \end{cases}$$ (5.26)

where $\sigma_N E$ is the current component due to uncondensed electrons. For $|E - E_T| \ll E_T$, that is E near the conduction threshold, the current is given by

$$\langle J(t)\rangle \sim (E - E_T)^\varsigma, E > E_T$$ (5.27)
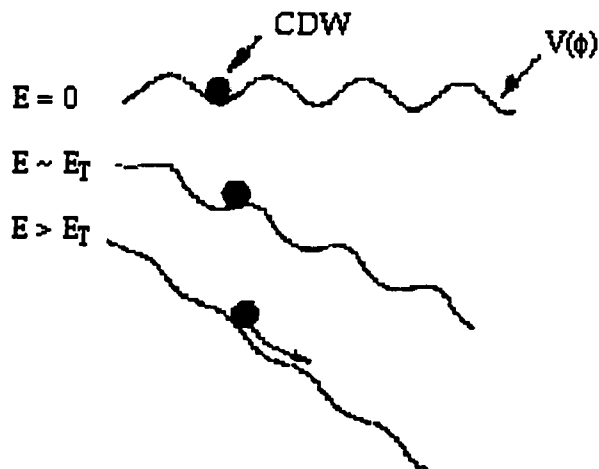
Figure 5.14: Single particle in a sinusoidal washboard potential model (From Ref. [36]).

with $\zeta = 1/2$. In the presence of multiple pinning centers, the mean field approximation can be used. In this approximation, each of a large number, N, of phases is coupled to all the others. In this case the current has a similar dependence on the voltage as in Eqn. 5.26 with $\zeta = 3/2$ [25].

Another important characteristic of charge density waves in metals is the observation of hysteresis in the I-V curve in some samples. Levy et al. point out in Ref. [56] that, the switching and hysteresis occur in the limits of strong pinning or large normal carrier resistance. The authors propose a model in which the CDW is coupled to a background of uncondensed electrons. Another model which gives a hysteretic I-V curve has been proposed by Strogatz et al. [84]. The authors calculated the time derivative of the phase using a hamiltonian with a coupling term periodic in the phase differences of the domains.

5.5.2   Wigner Solid

A system in which a spatially periodic charge density is formed as a result of electron-electron interactions is the Wigner Solid, which was predicted by Wigner in 1934 [92]. Three energy scales should be considered to understand the conditions for the formation of a 2-D Wigner solid:

- Characteristic potential energy per particle, V_c. This is the potential energy due to Coulomb Interaction of electrons, frozen in a triangular lattice configuration which minimizes the total energy.

$$V_c = \frac{e^2}{\epsilon a}, \tag{5.28}$$

where $a = \sqrt{\pi n}$ is the radius of the Wigner-Seitz cell of the triangular lattice, and ϵ is the dielectric constant.

- Thermal kinetic energy, $k_B T$.

- Fermi energy, E_F, the energy scale which represents the quantum fluctuations:

$$E_F = \frac{\hbar^2 \pi n}{m^*}. \tag{5.29}$$

The ratio of the potential energy and the thermal energy define a single dimensionless parameter, γ given by

$$\gamma = \frac{e^2 \sqrt{\pi}}{\epsilon k_B T} n^{1/2}. \tag{5.30}$$

For $\gamma \gg 1$ the system is ordered. For $\gamma \ll 1$ in is in a disordered phase. At a critical melting temperature, T_{mc}, the system undergoes a liquid-solid transition.

Another dimensionless parameter is the quantum ordering parameter, r_s, which is the ratio

$$r_s = \frac{V_c}{E_F} = \frac{e^2 m^*}{\epsilon \hbar^2 \sqrt{\pi n}} = \frac{a}{a_B}. \tag{5.31}$$

Here a_B is the Bohr radius. When r_s is very large, the electrons again order in a solid phase. As the density is increased, quantum fluctuations dominate and the crystal

melts. This transition is called the "Wigner transition". The density at which the melting occurs is called the critical density, and is given by

$$n_W = \left(\frac{e^2 m^*}{r_c^s \epsilon \hbar^2} \right)^2 . \qquad (5.32)$$

Monte Carlo calculations give $r_s^c \simeq 37$.

A strong magnetic field forms degenerate Landau Levels and localizes the particles by decreasing the overlap of the wavefunctions between the lattice points. Therefore, it can suppress quantum fluctuations and a Wigner solid may be formed, even if the density of the electrons is larger than the critical melting density, n_W, at $B = 0$. This is called a Magnetically Induced Wigner Solid (MIWS) and has been experimentally observed in *GaAs/AlGaAs* heterojunctions [4]. In the solid phase, the device has a very large resistance for small bias. As the voltage bias is increased, the current stays low until a threshold voltage, V_T, is reached. Beyond V_T, the current increases drastically. This behavior can be explained in terms of the depinning transition of charge density waves. It has been recently reported that for some magnetic field values, the I-V curve can exhibit multi-stability and hysteresis [93] as shown in Fig. 5.15.

5.5.3 Discussion

The comparison of Fig. 5.15 and Fig. 3.1 shows that, the I-V curves of the 200×200 arrays and those of the MIWS are strikingly similar. At nonzero temperatures, the low voltage part of the I-V curves can be very well fit with a hyperbolic sine function. Moreover, the dynamic critical exponents of CDW's and the quantum dot arrays have very similar values. In this section, these similarities will be investigated in more detail.

The experimental results for the MIWS system show that threshold field, $E_T \sim 250 mV cm^{-1}$ [93]. The threshold voltage, V_T, in the arrays is about $5mV$ (non-hysteretic regime) and the length of the array is about $160 \mu m$. Therefore, the threshold field is on the order of $300 mV cm^{-1}$, very close to the value in the MIWS. In the hysteretic regime, the current right after switching is on the order of $0.1 \mu A$ for both cases.
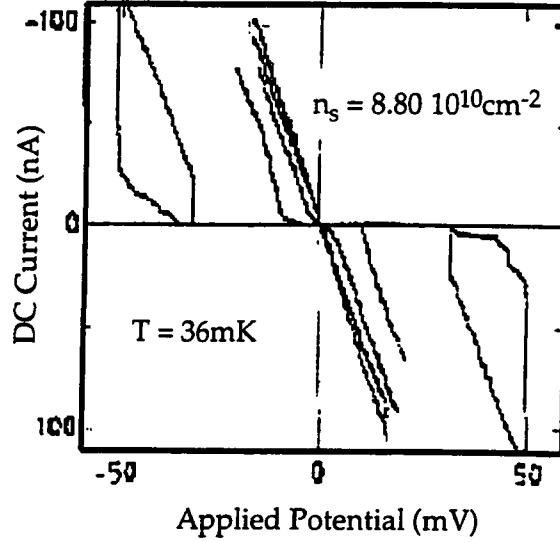
Figure 5.15: The I-V curve of an MIWS (From Ref. [4]).

At finite temperatures, and small electric fields, that is $E \ll E_T$, the current through the MIWS can be very well fit by

$$I(E) \sim \sinh(N_D e E a/T) e^{-(2N_D e E_T a/\pi T)} \qquad (5.33)$$

where N_D is the number of electrons in each crystal domain. The same functional dependence is found for the arrays as shown in Fig. 4.2 and discussed in Sec. 4.2.

The other striking similarity between the transport properties of the arrays and CDW's is reflected in the dynamical critical exponent, ζ, which gives the current in the vicinity of the conduction threshold. The theoretical values are $\zeta = 1/2$ (Eqn. 5.26) and $\zeta = 3/2$ for single and many particles in a washboard potential, respectively. The fits to the experimental results for the arrays and single dots give $\zeta \sim 1.5$ and $\zeta \sim 0.5$ (Chapter 4). The etched array can actually be thought of as a physical realization of multiple impurity sites, and a single dot as a single impurity site. It is then necessary to compare the potential and kinetic energies electrons in a single dot, to see whether a Wigner solid can form. The potential inside a dot can be approximated by a parabola with the harmonic oscillator energy, $\hbar\omega \sim 1meV$ [67].

The 2-DEG used in the experiments has a sheet density, $n_s \sim 3 \times 10^{11} cm^{-2}$. Assuming a dot radius of $100nm$, the number of electrons, N, in the dot can be estimated to be 100. The energy levels of a two dimensional harmonic oscillator are given by

$$E_{k,l} = \hbar\omega(k + l + 1/2). \tag{5.34}$$

The energy can be written alternatively as

$$E_n = \hbar\omega(n + 1/2), \tag{5.35}$$

each level being $2(n + 1)$ fold degenerate (including spin degeneracy). To find the Fermi energy, $E_F = E_{n=n_F}$, it is enough to solve the equation below for n_F:

$$N = 2\sum_{n=0}^{n_F}(n + 1) = 3n_F + n_F^2. \tag{5.36}$$

Then,

$$n_F = -\frac{3}{2} + \sqrt{\frac{9}{4} + N} \sim -\frac{3}{2} + \sqrt{N}. \tag{5.37}$$

Therefore, the Fermi energy is given by

$$E_F = \hbar\omega(-1 + \sqrt{N}) = 9\hbar\omega. \tag{5.38}$$

For $\hbar\omega \sim 1meV$ [67], the Fermi energy is about $10meV$, with $N = 100$. The potential energy, V_c, on the other hand can be estimated to be close to $10meV$, from Eqn. 5.28, with $\epsilon = 13.6$ [1], for $GaAs$. The ratio, r_s, of these two energies, is given by

$$r_s \sim \frac{e^2}{\epsilon\hbar\omega}\sqrt{\frac{\pi n}{N}}. \tag{5.39}$$

Since $n/N = 1/A$, where A is the area of the dot, r_s does not depend on the electron number but depends on the shape of the dot, namely its area and $\hbar\omega$. Both A and $\hbar\omega$ are adjusted by the gate in the structures studied here.

$$r_s \sim \frac{e^2\sqrt{\pi}}{\epsilon}\frac{1}{\hbar\omega\sqrt{A}}. \tag{5.40}$$

As the gate voltage becomes more negative, A decreases and $\hbar\omega$ increases.

The thermal energy at $20mK$ on the other hand, is less than $100\mu V$, so that the temperature is lower than the melting temperature of a Wigner Solid characterized by the above potential and kinetic energies.

A CDW model has been proposed by Field et al. [24] to explain the conductance oscillations in single quantum dots. Although the energy scales and exponents are very consistent with the formation of a Wigner Solid and therefore a CDW state, high frequency ($> 10MHz$) ac measurements should be done to see resonances corresponding to the vibrational modes of the electron lattice.

5.6   Order Parameters and Critical Exponents

The experimental results presented in Sec. 3.2.1, Sec. 3.2.3 and in Chapter 4 can be interpreted in terms of a second order phase transition with control parameters T, V_g, $V_{arr,dot}$ and order parameters differential conductance G, I_{ds} and ΔV_{ds}. In this section, they will be classified and their values will be presented. The relations which can be obtained from the data are:

$$I_{ds} = (V_{arr,dot} - V_T)^\varsigma \qquad (5.41)$$

$$\Delta V_{ds} = (T_0 - T)^\alpha \qquad (5.42)$$

$$\Delta V_{ds} = (V_{gT} - V_g)^\xi \qquad (5.43)$$

Eqn. 5.41 is valid for the non-hysteretic regime. Eqn. 5.42 and Eqn. 5.43 on the other hand are valid for the hysteretic regime. Table 5.1 presents the experimental and theoretical values.

As mentioned in Chapter 4, ς for the array and single dot are very consistent with the theoretical values obtained for charge density waves. ς for the array is also close to the 5/3 value estimated by Middleton and Wingreen [72]. The discrepency can be related to the range of the fit or more possibly to the size of the array. In [72] the authors state that the array size should be larger than 400×400 to measure the correct exponent.

Dimension	Exponent	Experiment	CDW [35]	Percolation [72]
2 (array)	ζ	1.55	3/2	5/3
	α	0.57		
	ξ	> 1		
0 (dot)	ζ	0.52	1/2	1 (1-D array)
	α			
	ξ	< 1		

Table 5.1: Critical exponents.

α for the single dot is significantly different from that for the array. Although there are not many data points available for the single dot, it can be clearly seen from Fig. 3.13 that it is larger than one (concave down). For the arrays, $\alpha < 1$ from Fig. 3.2 and other fits not presented in the dissertation. The difficulty here comes from the merging and dissociation of the multiple loops. It is hard to trace a single loop as a function of the gate voltage. Therefore the fits give numbers ranging from 1.3 to 2.3.

Finally, ζ for the array is 0.57. The value for the single dot is not available since its temperature dependence was very weak up to $700mK$.

Chapter 6

Conclusions

6.1   Summary of Contributions

This dissertation has made several contributions to the understanding of low temperature electron transport in quantum dot arrays and to their fabrication.

- I have designed and fabricated 200 × 200 quantum dot arrays using MBE, e-beam lithography and etching. These devices constitute the first large 2-D semi-conducting arrays which can be driven into the Coulomb blockade regime at low temperatures. This is achieved by changing the voltage on the gate covering the device.

- I have measured these devices in a dilution refrigerator, typically at 20mK, and observed, for the first time, multiple switching and hysteresis in the I-V curves. I experimentally investigated these quantum dot array multi-stabilities for the first time, as a function of the gate voltage, temperature and magnetic field.

- I investigated the dynamical critical behavior of the arrays and control devices in the non-hysteretic regime. I showed the power law dependence of the current on the applied voltage, and obtained the critical exponents.

- I designed and fabricated a top gated three lead single dot, to study the effect of gate leakage in the etched arrays and single control devices.

The studies in this thesis resulted in a large amount of data about the I-V curves of arrays and the multi-stabilities they contain. All the essential parts of it are presented in this dissertation. However, in spite of the efforts in this thesis and those of other groups, the microscopic cause of the hysteresis and multi-stability is currently unknown. The possible models range from transport through higher order subbands in *GaAs* [76], electron heating [32], gate leakage [44] and impurities [11], to the formation of a Charge Density Wave state [35]. Time will show us which one of these, or another model is correct.

6.2 Future Experiments

As device sizes decrease due to developments in fabrication techniques, the quantum confinement and single electron charging effects will become more and more significant. The observation of these effects at room temperature has already been reported [65].

I think, the increasing efforts for making useful single electron devices will increase the importance of the non-linear regime. In my opinion, the very next steps in research should be:

- Detailed study of the hysteresis, and the clarification of the underlying mechanism.

- Experimental study of the three lead single dot in the Coulomb blockade regime as a function of the transparency of the third lead.

- Fabrication of more uniform arrays by using dry etching techniques and higher mobility 2-DEG structures.

- Detailed study of disorder and its significance in the experimental results presented in this dissertation.

- More detailed investigation of the critical exponents and order parameters, in particular, their dependence on the temperature, gate voltage, array size and array dimension.

- Study of arrays with various sizes and dimensions. In particular, the transition from quasi 1-D to quasi 2-D.

- More detailed study of the hierarchy of switching events.

- High frequency *ac* measurements. These measurements are very powerful and useful in making a definitive statement about the underlying mechanism for the hysteresis. The main difficulty is the efficient coupling of the *ac* signal to the device. I think this is just a practical problem which can be overcome by properly designed wiring and a waveguide system.

Again the time will give the answers to all the questions above. It will be exciting to wait and see...

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Appendix A

Experimental Setups

This appendix gives the experimental setups for the measurements described in Sec. 5.2.
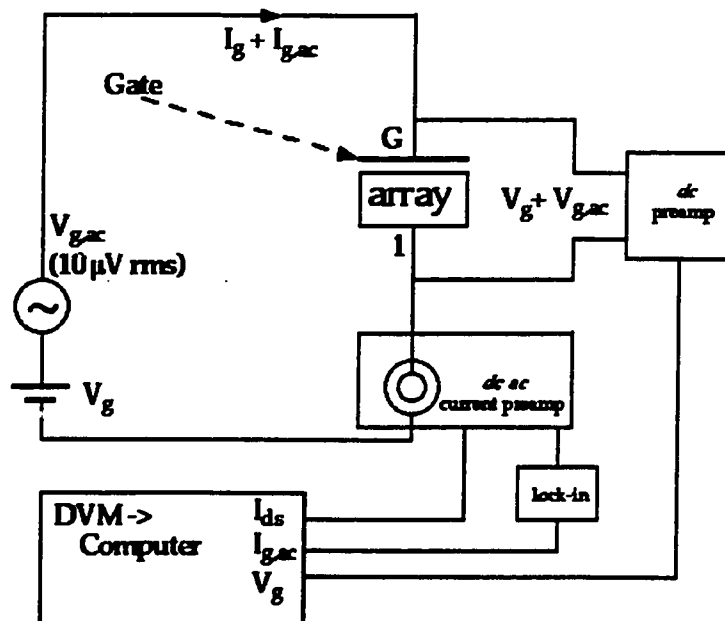
Figure A.1: The experimental setup for the $4.2K$ gate current measurements.
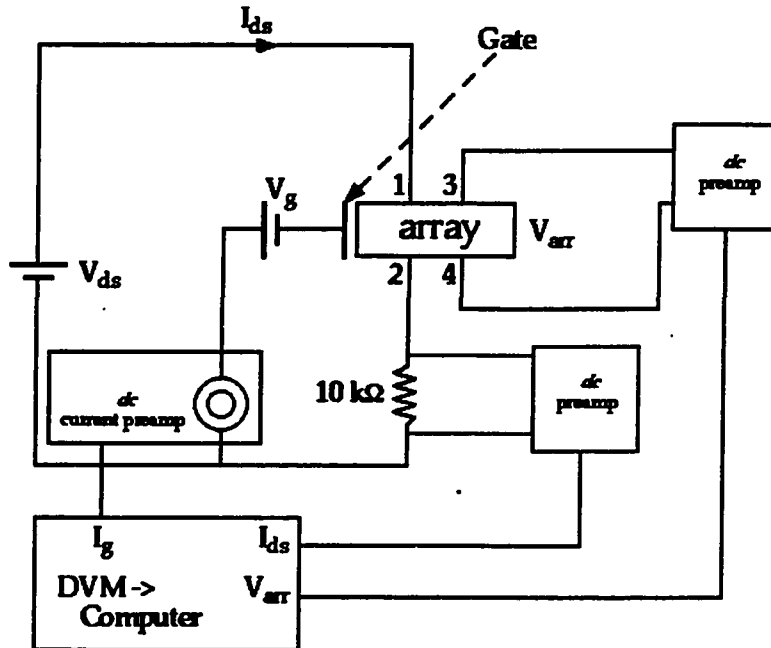
Figure A.2: The experimental setup for the $40mK$ gate current measurements.

Appendix B

MBE Growth Files

In this Appendix, the MBE growth files used to grow the 2-DEG strucutres are given. In these files, `subramp2.8.g` is a subroutine which increases the substrate temperature to $700C$ and then decreases it to $660C$ after waiting ten minutes. The *As* shutter is opened in this subroutine before reaching $400C$.

The subroutine `100per.g` contains 10 subroutines `10per.g` which contains 10 subroutines `1per.g`. The last one has the lines

```
wait 13.90
shutter 5Al o 30.61
```

In the growth file, the letters o and c give the commands "open" and "close", respectively. The temperatures are in degrees Celcius and all the other numbers represent the time interval in seconds during which the command is executed. In particular, the second line in the above subroutine means that the Al shutter is kept open for 30.61 seconds, in other words, it was closed at the end of that time interval. If no time is specified after o or c, the shutter preserves its state until it gets the opposite command.

B.1   *Device 1, 2, 3, 4*

```
print begin growth 2630:


#      · GR[4Ga] = 0.575 um/hr,
#        GR[5Al] = 0.297 um/hr, (x=0.34)
#        2-DEG SL Buffer
#        300 A spacer, 5s interrupt, 3.5e18 (170A), 300 A cap, SL
#
#              300 A GaAs            i
#              170 A AlGaAs x=0.34   n(Si)=3.5e18(129.32 W)
#              300 A AlGaAs x=0.34   i
#      5 s interrupt
#            10000 A GaAs            i
#              500 A AlGaAs x=0.34   i
#            13000 A SL: 100A AlGaAs i (100 periods)
#                         30A    GaAs i
#             3000 A GaAs            i
#              sub.   GaAs           SI
#


settemp 8As 323.20
settemp 4Ga 1004.00
settemp 5Al 1350.00
#settemp 1Si 1318.31
settemp sub idle
print $ Put 2As, 4Ga, 5Al, 1Si, sub in remote.
print $ Make sure 1Si is on high, and ready.
print $ Turn off Ti-ball and ion-gauges.
print $ Face sub towards sources, set rotation to 8 rpm.
pause
```

```
include ug/subramp.2.8.g
shutter 2As c
settemp sub 660
wait 180
settemp sub 640
wait 600
shutter 4Ga o
wait 1878.26
include g/100per.g
shutter 5Al o 206.42
wait 6260.87
shutter 4Ga c
wait 5
shutter 5Al o
shutter 4Ga o
wait 123.85
shutter 1Si o 70.18
shutter 5Al c
wait 187.83
shutter 4Ga c
settemp sub idle
#settemp 1Si idle
wait 300
shutter 8As c
print 4Ga, 1Si and 5Al at growth temperatures
print end growth #2630
```

B.2   *Shallow Device*

```
print begin growth 2631:


#      GR[4Ga] = 0.575 um/hr,
#      GR[5Al] = 0.297 um/hr, (x=0.34)
#      2-DEG SL Buffer
#      300 A spacer, 5s interrupt, 2.8e18 (170A), 300 A cap, SL
#
#             300 A GaAs            i
#             170 A AlGaAs x=0.34   n(Si)=2.8e18(126.81 W)
#             300 A AlGaAs x=0.34   i
#      5 s interrupt
#           10000 A GaAs            i
#             500 A AlGaAs x=0.34   i
#           13000 A SL: 100A AlGaAs i (100 periods)
#                         30A   GaAs i
#            3000 A GaAs            i
#            sub.   GaAs            SI
#


settemp 8As 323.20
settemp 4Ga 1004.00
settemp 5Al 1350.00
#settemp 1Si 1318.31
settemp sub idle
print $ Put 2As, 4Ga, 5Al, 1Si, sub in remote.
print $ Make sure 1Si is on high, and ready.
print $ Turn off Ti-ball and ion-gauges.
print $ Face sub towards sources, set rotation to 8 rpm.
pause
```

```
include ug/subramp.2.8.g
shutter 2As c
settemp sub 660
wait 180
settemp sub 640
wait 600
shutter 4Ga o
wait 1878.26
include g/100per.g
shutter 5Al o 206.42
wait 6260.87
shutter 4Ga c
wait 5
shutter 5Al o
shutter 4Ga o
wait 123.85
shutter 1Si o 70.18
shutter 5Al c
wait 187.83
shutter 4Ga c
settemp sub idle
#settemp 1Si idle
wait 300
shutter 8As c
settemp 8As idle
settemp 4Ga idle
settemp 5Al idle
#print 4Ga, 1Si and 5Al at growth temperatures
print end growth #2631
```

B.3   Three Lead Dot

```
print begin growth #2385:


#       GR[4Ga] = 0.838 um/hr,
#       GR[5Al] = 0.430 um/hr, (x=0.34)
#       2-DEG SL Buffer
#       100 A spacer, 5s interrupt, 1.0e18 (170A), 100 A cap, SL
#
#               100 A GaAs           i
#               400 A AlGaAs x=0.34  n(Si)=1.0e18(129.32 W)
#               400 A AlGaAs x=0.34  i
#       5 s interrupt
#             10000 A GaAs           i
#               500 A AlGaAs x=0.34  i
#             13000 A SL: 100A AlGaAs i (100 periods)
#                         30A   GaAs i
#              3000 A GaAs           i
#              sub.   GaAs           SI
#


settemp 2As 306.00
settemp 4Ga 987.19
settemp 5Al 1325.06
settemp 1Si 1261.40
settemp sub idle
print $ Put 2As, 4Ga, 5Al, 1Si, sub in remote.
print $ Make sure 1Si is on high, and ready.
print $ Turn off Ti-ball and ion-gauges.
print $ Face sub towards sources, set rotation to 8 rpm.
pause
```

```
include ug/subramp.2.8.g
shutter 2As c
settemp sub 640
wait 300
shutter 4Ga o
wait 1288.78
include g/100per.g
shutter 5Al o 141.96
wait 4295.94
shutter 4Ga c
wait 5
shutter 5Al o
shutter 4Ga o
wait 113.56
shutter 1Si o 113.56
shutter 5Al c
wait 42.96
shutter 4Ga c
settemp sub idle
settemp 1Si idle
wait 300
shutter 2As c
print end growth #2385
```

Appendix C

Weak Localization in the Array

Mesoscopic effects such as universal conductance fluctuations and weak localization appear due to the interference from multiple conduction paths through the sample. The most important condition for the observation of these effects is, therefore, an electron phase which is preserved during transport. The characteristic time over which the phase coherence is lost is defined as the "phase breaking time" τ_ϕ, and $\gamma_\phi = 1/\tau_\phi$ is called the "phase breaking" rate. Phase breaking and conductance fluctuations are extensively studied using single quantum dots [61, 64, 63, 17]. Both structures whose classical scattering are regular (non-chaotic) and chaotic have been studied [62].

Weak localization, in chaotic versus non-chaotic cavities, on the other hand, has been experimentally studied by Chang et al. [15]. The authors studied arrays containing circular and stadium shaped individual dots. They found a lorentzian and a triangular lineshape for the chaotic and non-chaotic structures, respectively. The same measurement can be repeated using the arrays in this thesis. A measurement of the longitudinal resistance R_L of the array as a function of the magnetic field and gate voltage was made at $40mK$ (Fig. C.1). The individual dots in this case are rectangular in design but because of lateral depletion, they have a circular shape. As expected, the lineshape around $B = 0$ is a triangle (non-chaotic).

It is also possible to see the resistance peak around $B = 0.2T$ which is due to the first order electron pinball orbit [91]. The periodic array of scatterers in this case are
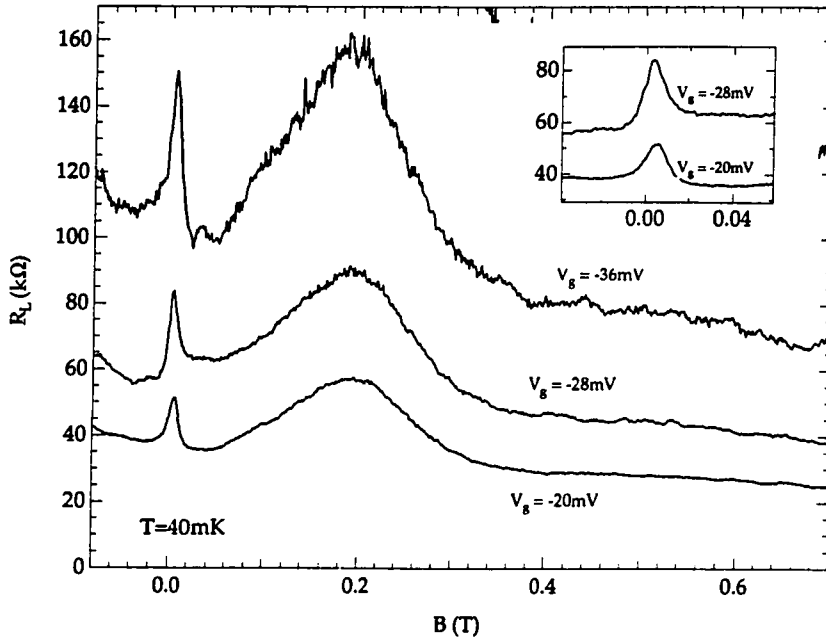
Figure C.1: The longitudinal resistance of the array (*Device 2*) versus the magnetic field for various gate voltages.

the etched plus sign regions. The diameter, a, of the orbit at a given magnetic field, B, can be found from classical physics as

$$a = \frac{2m^* v_F}{eB},$$ (C.1)

where m^* and v_F are the effective mass and the Fermi velocity of the electron, respectively. Assuming a sheet electron density $n_s = 3 \times 10^{11} cm^{-2}$ and $B = 0.2T$, a can be obtained as $810 nm$ which is very close to the period of the plus sign pattern. This is a very good confirmation for the efficiency of the etching technique in isolating and defining the dots.

Appendix D

Computer Code

Below is the code used to calculate the I-V curve and the differential conductance of a triple junction system. It is a "Procedure" written in "IgorPro" software which runs on a macintosh computer.

```
|||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||
||||||||
||||||||         GateMacro calculates the G-Vg curve of a single dot with three leads
||||||||      at finite temperature.  Makes the initializations, and plots the graphs
||||||||
|||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||

Macro GateMacro(Nem, TempItm, deltaTm, Vgm, Vdsm, VgPoints, T)
    Variable/D Nem, TempItm, deltaTm, Vgm, Vdsm, VgPoints, T, C1M, C2M, C3M, R1M, R2M, R3M
    Prompt Nem, "Enter the max number of electrons"
    Prompt TempItm, "Enter the number of time iterations"
    Prompt deltaTm, "Enter the infinitesimal time interval"
    Prompt Vgm, "Enter the maximum gate voltage"
    Prompt Vdsm, "Enter the source drain voltage"
    Prompt VgPoints, "Enter the number of data points for the gate voltage"
    Prompt T, "Enter the temperature in units of Csigma"

    Redimension/N=(2*Nem+1) Number
    Redimension/N=(2*Nem+1) sigma
    Redimension/N=(2*Nem+1) sigmaPrev
    Redimension/N=(2*Nem+1) G1p
    Redimension/N=(2*Nem+1) G2p
    Redimension/N=(2*Nem+1) G3p
    Redimension/N=(2*Nem+1) G1m
    Redimension/N=(2*Nem+1) G2m
    Redimension/N=(2*Nem+1) G3m
    Redimension/N=(2*Nem+1) dummy
```

111

```
        Redimension/N=(2*Vgpoints+1) Vg
        Redimension/N=(2*Vgpoints+1) conductance
        Redimension/N=(3) Ids


||||||
||||||         One set of numbers is C1 = 1.5, C2 = 1.2, C3 = 10, and resistors, 100,10000,10000
||||||       Likharev set of numbers:  C1 = 0.8, C2 = 0.8, C3 = 0,  100,1000, R3 G3pm= 0
||||||
        C1M = 1.5 | C: in units of 10-16, e:  iuo 10-19, R: iuo 1000, V: iuo mV, G: iuo 1/psec
        C2M = 1.2
        C3M = 10
        R1M = 100
        R2M = 100
        R3M = 10000


        GVgTrace(Nem, TempItm, deltaTm, Vgm, Vdsm, C1M, C2M, C3M, R1M, R2M, R3M, VgPoints,T)
        GVgCurve(Vgm, C1M, C2M, C3M, R1M, R2M, R3M)
EndMacro


||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||
||||||
||||||         GVgTrace traces the G-Vgcurve, calculates G for various values of Vg by calling SigmaInt
||||||       for every voltage value.  Sigma Int calculates sigma for given voltages and calculates the current
||||||       afterwards.  Then GVgTrace takes the slope at the origin to get the conductance.
||||||
||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||
Function /D GVgTrace(Ne, TempIt, deltaT, Vgmax, Vds, C1, C2, C3, R1, R2, R3, Vpts, T)
        Variable/D Ne, TempIt, deltaT, Vgmax, Vds
        Variable/D R1, R2, R3, C1, C2, C3, Vpts, T
        Variable /D Nmax, DeltaV, NVmax, Voltage
        Variable n,m
        Nmax = Ne*2 + 1
        NVmax = Vpts*2 + 1


||||||
||||||         Initialize sigma (The probability distribution)
||||||
        n = 0
            do
                sigma[n] = 0
                Number[n] = n - Ne
                n = n +1
            while (n < Nmax)
        sigma[(Nmax-1)/2 ]=1


        DeltaV = 0
```

```
if (Vpts > 0)
    DeltaV = Vgmax/Vpts
endif
Voltage = -Vgmax
n = 0
    do
        Vg[n] = Voltage
        Ids[0] = SigmaInt(Ne, TempIt, deltaT, Voltage, (-Vds), C1, C2, C3, R1, R2, R3, T)
        Ids[2] = SigmaInt(Ne, TempIt, deltaT, Voltage, Vds, C1, C2, C3, R1, R2, R3, T)
        Ids[1] = 0
        conductance[n] = 0.00001*6.67*(Ids[2] - Ids[0])/(2*Vds*2*2.56)
        n = n + 1
        Voltage = Voltage + DeltaV
    while (n < NVmax)
Return (NVmax)
End
```

```
||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||
||||||
||||||        "SigmaMacro" calculates the I-V curve of a single dot with three leads
||||||    at finite temperature, as a function of the gate voltage
||||||    SigmaMacro makes the initializations, and plots the graphs
||||||
||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||
Macro SigmaMacro(Nem, TempItm, deltaTm, Vgm, Vdsm, VPoints, T)
    Variable/D Nem, TempItm, deltaTm, Vgm, Vdsm, VPoints, T, C1M, C2M, C3M, R1M, R2M, R3M
    Prompt Nem, "Enter the max number of electrons"
    Prompt TempItm, "Enter the number of time iterations"
    Prompt deltaTm, "Enter the infinitesimal time interval"
    Prompt Vgm, "Enter the gate voltage"
    Prompt Vdsm, "Enter the maxiumum source drain voltage"
    Prompt VPoints, "Enter the number of data points"
    Prompt T, "Enter the temperature in units of Csigma"

    Redimension/N=(2*Nem+1) Number
    Redimension/N=(2*Nem+1) sigma
    Redimension/N=(2*Nem+1) sigmaPrev
    Redimension/N=(2*Nem+1) G1p
    Redimension/N=(2*Nem+1) G2p
    Redimension/N=(2*Nem+1) G3p
    Redimension/N=(2*Nem+1) G1m
    Redimension/N=(2*Nem+1) G2m
    Redimension/N=(2*Nem+1) G3m
    Redimension/N=(2*Nem+1) dummy
    Redimension/N=(2*Vpoints+1) Vds
    Redimension/N=(2*Vpoints+1) Ids
```

```
||||||
||||||          One set of numbers is C1 = 1.5, C2 = 1.2, C3 = 10, and resistors, 100,10000,10000
||||||       Likharev set of numbers:  C1 = 0.8, C2 = 0.8, C3 = 0, 100,1000, R3 G3pm= 0
||||||
    C1M = 0.8 | C: in units of 10~16, e:  iuo 10~19, R: iuo 1000, V: iuo mV, G: iuo 1/psec
    C2M = 0.8
    C3M = 0
    R1M = 100
    R2M = 1000
    R3M = 100000
    IVTrace(Nem, TempItm, deltaTm, Vgm, Vdsm, C1M, C2M, C3M, R1M, R2M, R3M, Vpoints,T)


||||||
||||||          The two lines below are for calculating the probability density only
|          SigmaInt(Nem, TempItm, deltaTm, Vgm, Vdsm, C1M, C2M, C3M, R1M, R2M, R3M)
|          ProbDist(Nem, C1M, C2M, C3M, R1M, R2M, R3M)
||||||
    IVCurve(Vdsm, C1M, C2M, C3M, R1M, R2M, R3M)
EndMacro


|||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||
||||||
||||||          IVTrace traces the I-V curve, calculates I for various values of Vds by calling SigmaInt
||||||       for every voltage value.  Sigma Int calculates sigma for given voltages and calculates the current
||||||       afterwards.
||||||
|||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||
Function /D IVTrace(Ne, TempIt, deltaT, Vg, Vdsmax, C1, C2, C3, R1, R2, R3, Vpts, T)
    Variable/D Ne, TempIt, deltaT, Vg, Vdsmax
    Variable/D R1, R2, R3, C1, C2, C3, Vpts, T
    Variable /D Nmax, DeltaV, NVmax, Voltage
    Variable n,m
    Nmax = Ne*2 + 1
    NVmax = Vpts*2 + 1


|||||||||          Initialize sigma (The probability distribution)
    n = 0
        do
            sigma[n] = 0
            Number[n] = n - Ne
            n = n +1
        while (n < Nmax)
    sigma[(Nmax-1)/2 ]=1

    DeltaV = 0
    if (Vpts > 0)
        DeltaV = Vdsmax/Vpts
```

```
        endif
        Voltage = -Vdsmax
        n = 0
        do
                Ids[n] = SigmaInt(Ne, TempIt, deltaT, Vg, Voltage, C1, C2, C3, R1, R2, R3, T)
                Vds[n] = Voltage
                n = n + 1
                Voltage = Voltage + DeltaV
            while (n < NVmax)


                Below is for a back sweep
 |      n = NVmax
 |          do
 |                Ids[n] = SigmaInt(Ne, TempIt, deltaT, Vg, Voltage, C1, C2, C3, R1, R2, R3, T)
 |                Vds[n] = Voltage
 |                n = n + 1
 |                Voltage = Voltage - DeltaV
 |          while (n < 2*NVmax)

        Return (NVmax)
        End



                SigmaInt calculates the probability distribution and the
            current for the given voltage, and temperature

Function /D SigmaInt(Ne, TempIt, deltaT, Vg, Vds, C1, C2, C3, R1, R2, R3, T)
        Variable/D Ne, TempIt, deltaT, Vg, Vds, T
        Variable/D R1, R2, R3, C1, C2, C3
        Variable /D Nmax, sigmanm1, sigman, dum1, Csigma, e, Current, temperature, bet
        Variable n,m
        Nmax = Ne*2 + 1
        e = 1.6


        Csigma = C1 + C2 + C3
        temperature = (e*e*T)/Csigma

        dum1 = (10/(e*R1*Csigma))*(-e/2+(-(n-Ne)*e + C3*Vg + (C2 + C3/2)*Vds))
        G1p[n] = dum1/(1-exp(-((-e/2+(-(n-Ne)*e + C3*Vg + (C2 + C3/2)*Vds))*e)/(Csigma*T)))
        dum1 = (10/(e*R2*Csigma))*(-e/2+(-(n-Ne)*e + C3*Vg - (C1 + C3/2)*Vds))
        G2p[n] = dum1/(1-exp(-((-e/2+(-(n-Ne)*e + C3*Vg - (C1 + C3/2)*Vds))*e)/(Csigma*T)))
        dum1 = (10/(e*R3*Csigma))*(-e/2+(-(n-Ne)*e - (C1+C2)*Vg - (C2/2-C1/2)*Vds))
        G3p[n] = dum1/(1-exp(-((-e/2+(-(n-Ne)*e - (C1+C2)*Vg - (C2/2-C1/2)*Vds))*e)/(Csigma*T)))
        dum1 = (10/(e*R1*Csigma))*(-e/2-(-(n-Ne)*e + C3*Vg + (C2 + C3/2)*Vds))
```

```
         G1m[n] = dum1/(1-exp(-((-e/2-(-(n-Ne)*e + C3*Vg + (C2 + C3/2)*Vds))*e)/(Csigma*T)))
         dum1 = (10/(e*R2*Csigma))*(-e/2-(-(n-Ne)*e + C3*Vg - (C1 + C3/2)*Vds))
         G2m[n] = dum1/(1-exp(-((-e/2-(-(n-Ne)*e + C3*Vg - (C1 + C3/2)*Vds))*e)/(Csigma*T)))
         dum1 = (10/(e*R3*Csigma))*(-e/2-(-(n-Ne)*e - (C1+C2)*Vg - (C2/2-C1/2)*Vds))
         G3m[n] = dum1/(1-exp(-((-e/2-(-(n-Ne)*e - (C1+C2)*Vg - (C2/2-C1/2)*Vds))*e)/(Csigma*T)))


||||||
|||||||          Below gives the tunneling rates at zero temperature
|        G1p[n] = (10/(e*R1*Csigma))*(-e/2+(-(n-Ne)*e + C3*Vg + (C2 + C3/2)*Vds))
|        if (G1p[n] < 0)
|            G1p[n] = 0
|        endif
|        G2p[n] = (10/(e*R2*Csigma))*(-e/2+(-(n-Ne)*e + C3*Vg - (C1 + C3/2)*Vds))
|        if (G2p[n] < 0)
|            G2p[n] = 0
|        endif
|        G3p[n] = (10/(e*R3*Csigma))*(-e/2+(-(n-Ne)*e - (C1+C2)*Vg - (C2/2-C1/2)*Vds))
|        if (G3p[n] < 0)
|            G3p[n] = 0
|        endif
|        G1m[n] = (10/(e*R1*Csigma))*(-e/2-(-(n-Ne)*e + C3*Vg + (C2 + C3/2)*Vds))
|        if (G1m[n] < 0)
|            G1m[n] = 0
|        endif
|        G2m[n] = (10/(e*R2*Csigma))*(-e/2-(-(n-Ne)*e + C3*Vg - (C1 + C3/2)*Vds))
|        if (G2m[n] < 0)
|            G2m[n] = 0
|        endif
|        G3m[n] = (10/(e*R3*Csigma))*(-e/2-(-(n-Ne)*e - (C1+C2)*Vg - (C2/2-C1/2)*Vds))
|        if (G3m[n] < 0)
|            G3m[n] = 0
|        endif
|||||||
         G3m[n] = 0 |These are set to zero for standard
         G3p[n] = 0 |(non gate leakage) single dot, and commented for gate leakage.
             n = n+1
         while (n < Nmax)


|||||||
|||||||          Forward time calculation of sigma is below.  this version is unstable for large T so it is
|||||||   more useful for studying time evolution in a small time interval.  Unnecessary iterations
|||||||   to look at steady state.
|||||||
|||||||
|||||||   Outer loop for time integration for all sigma
|    m = 0
|        do
```

```
|                sigmanm1 = sigma[0]
|                sigman = sigma[1]
|
||||||         Inner loop for calculating all sigma[n]'s for that time iteration
|                n = 1
|                    do
|     sigma[n] = (G1p[n-1] + G2p[n-1] + G3p[n-1])*sigmanm1*deltaT
|     sigma[n] = sigma[n] + (G1m[n+1] + G2m[n+1] + G3m[n+1])*sigma[n+1]*deltaT
|     sigma[n] = sigma[n] - (G1p[n] + G2p[n] + G3p[n]+G1m[n] + G2m[n] + G3m[n])*sigman*deltaT
|     sigma[n] = sigma[n] + sigman
|     sigmanm1 = sigman
|     sigman = sigma[n+1]
|                      n = n+1
|                    while (n < Nmax - 1)
|                m = m + 1
|        while (m < TempIt)
||||||
||||||
||||||          backward time version of the calculation of sigma is below
||||||      (Numerical Recipies, by Press et Al, p 43)
||||||
     m = 0
     do
         sigmaPrev = sigma
         bet = 1 + deltaT*(G1p[1] + G2p[1] + G3p[1]+G1m[1] + G2m[1] + G3m[1])
         sigma[1] = sigmaPrev[1]/bet
         n = 2
         do
dummy[n] = - deltaT*(G1m[n] + G2m[n] + G3m[n])/bet
bet=1+deltaT*(G1p[n]+G2p[n]+G3p[n]+G1m[n]+G2m[n]+G3m[n])+deltaT*(G1p[n-1]+G2p[n-1]+G3p[n-1])*dummy[n]
if (bet == 0)
Print "ERROR IN THE PROCEDURE: TRIDAG FAILED"
endif
sigma[n] = (sigmaPrev[n] + deltaT*(G1p[n-1] + G2p[n-1] + G3p[n-1])*sigma[n-1])/bet
n = n+1
         while (n < Nmax -1)
         n = Nmax -3
         do
         sigma[n] = sigma[n] - dummy[n+1]*sigma[n+1]
         n = n-1
         while (n > 0)

         m = m + 1
     while (m < TempIt)


||||||||        the loop below calculates the current from the sigma values
     Current = 0
```

```
        n = 0
            do
                Current = Current + (G2p[n] - G2m[n])*sigma[n]
                n = n +1
            while (n < Nmax - 1)
        Current = Current*(-1.6e+5) |Current in pA (Gamma in 1/psec, -19 +12 +12 = 5 exponent here)
    Return (Current)
    End


||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||
|||||||
|||||||          ProbDist
|||||||      The graph below plots sigma versus the number
|||||||
||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||
Window ProbDist(Nelec, C1P, C2P, C3P, R1P, R2P, R3P) : Graph
    Variable/D Nelec, C1P, C2P, C3P, R1P, R2P, R3P
    PauseUpdate; Silent 1 | building window...
    Display /W=(5,42,501,309) sigma vs Number
    ModifyGraph tick=2
    ModifyGraph mirror=1
    ModifyGraph fSize=16
    Label left "sigma(n,t)"
    Label bottom "n"
    SetAxis bottom -Nelec,Nelec
    SetAxis left 0,1
    EndMacro


||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||
|||||||
|||||||          The graph below plots the I-V curve
|||||||
||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||
Window IVCurve(Vmax, C1P, C2P, C3P, R1P, R2P, R3P) : Graph
    Variable/D Vmax, C1P, C2P, C3P, R1P, R2P, R3P
    PauseUpdate; Silent 1 | building window...
    Display /W=(5,42,501,309) Ids vs Vds
    ModifyGraph tick=2
    ModifyGraph mirror=1
    ModifyGraph fSize=16
    Label left "IBds (pA)"
    Label bottom "VBds (mV)"
    SetAxis bottom -Vmax,Vmax
EndMacro


||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||
|||||||
```

```
||||||        The graph below plots the G-Vg curve
||||||
|||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||
Window GVgCurve(Vmax, C1P, C2P, C3P, R1P, R2P, R3P) : Graph
    Variable/D Vmax, C1P, C2P, C3P, R1P, R2P, R3P
    PauseUpdate; Silent 1 | building window...
    Display /W=(5,42,501,309) conductance vs Vg
    ModifyGraph tick=2
    ModifyGraph mirror=1
    ModifyGraph fSize=16
    Label left "G (e2/h)"
    Label bottom "Vg (mV)"
    SetAxis bottom -Vmax,Vmax
EndMacro
```